JEDEC STANDARD

Isothermal Electromigration Test Procedure

JESD61A.01

(Revision of JESD61A, May 2007)

OCTOBER 2007

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2007
2500 Wilson Boulevard
Arlington, VA 22201-3834

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications at www.jedec.org

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE

Contents

Foreword ... iii
Introduction ... iii
1 Scope ... 1
2 Normative references ... 1
3 Terms and definitions ... 2
4 Symbols ... 4
5 Technical requirements ... 4
5.1 Equipment requirements ... 6
5.2 Test configuration ... 6
6 The isothermal test algorithm ... 7
6.1 Initialization phase ... 8
6.1.1 Measure the resistance at chuck temperature ... 8
6.1.2 Convert TCR (T_{ref}) to TCR(T_{chuck}) ... 9
6.1.3 Initial current value and current multiplication factor ... 9
6.1.4 Control loop to measure the initial thermal resistance ... 11
6.1.5 Instrument range and voltage compliance for the initialization phase ... 11
6.1.6 Temporary failure criterion for the initialization phase ... 11
6.1.7 Determination of the initial thermal resistance ... 12
6.2 Temperature staircase and convergence phases ... 12
6.2.1 Calculate the temperature step and the staircase temperature limit ... 14
6.2.2 Instrument range and voltage compliance for staircase/convergence/stress phases ... 14
6.2.3 Control loop for the temperature staircase and convergence phases ... 14
6.2.4 Temporary failure criteria for staircase and convergence phases ... 17
6.3 Stress phase ... 18
6.3.1 Set the power and the initial current at target stress temperature ... 19
6.3.2 Calculate the dependence of the resistance on the effective applied power ... 19
6.3.3 Control loop to maintain a constant stress temperature ... 19
6.3.4 Failure criterion for the stress phase ... 20
6.4 Exit at failure of the test line ... 21
6.4.1 Calculate the time-to-failure (TTF) ... 21
6.4.2 Required data report ... 22
6.4.3 Optional data report ... 22
6.4.4 Optional log file ... 22
6.5 Isothermal test characteristics ... 23
6.6 Example of isothermal test ... 24

ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE

Contents (cont'd)

7 Interferences 26
7.1 Measurement and control of the wafer temperature 26
7.2 Variation in TCR value 26
7.3 Resistance measurements 27
7.4 Feedback cycle time 27
7.5 Temperature gradients 28
7.6 Normalization of stress current density 29
7.7 Constant Current Test 29
Annex A (normative) ISOT convergence algorithm 30
Annex B (normative) Evaluation of the damage during the initial settling time 32
Annex C (informative) Bibliography 35
Annex D (informative) Differences between JESD61A.01 and JESD61A 36
Index 37

Tables

Table 1 – ISOT input parameters for a copper damascene line 24
Table A.1 – Predicted temperature steps in the convergence phase 30
Table A.2 – Calculated temperature steps in the convergence phase 31
Table B.1 – Calculation of the fractional damage 33
Table B.2 – Dependence of t_{corr} on E_a and n 34

Figures

Figure 1 – Measurement phases of the isothermal test 7
Figure 2 – Flow chart for ISOT initialization phase 10
Figure 3 – Flow chart for ISOT temperature staircase and convergence phases 13
Figure 4 – Flow chart for ISOT stress phase 18
Figure 5 – Flow chart for ISOT exit-at-failure phase 21
Figure 6 – ISOT temperature behavior 24
Figure 7 – ISOT resistance behavior 25
Figure 8 – ISOT thermal resistance behavior 25

Foreword

The isothermal test is an accelerated electromigration test performed on microelectronic metallizations. In the isothermal test, an attempt is made to maintain a constant mean temperature of the line under test, by varying the stress current and hence the amount of Joule heating imparted to the line.

Given a known and unvarying thermal resistance of the sample to the ambient, the isothermal test uses a feedback control to maintain a constant power dissipated in the metallization under test, so that a constant test line mean temperature is achieved. When the line resistance changes during the test, due to electromigration damage, the power is kept constant, by varying the stress current.

This document presents an algorithm for conducting the isothermal test using computer-controlled instrumentation. The intent is to provide a complete description of a functional isothermal test algorithm that will allow a programmer to implement and start using an accelerated electromigration test with ease. The algorithm is derived from published and unpublished literature. Bibliographic references are listed in Annex C.

This standard was formulated under the cognizance of JC-14.2 Committee on Wafer-Level Reliability and approved by the JEDEC Board of Directors (BoD) Ballot JCB-07-20. It was prepared with the contribution of the National Research Council of Italy, Institute for Microelectronics and Microsystems (CNR-IMM) of Bologna, Italy.

The present revision JESD61A introduces significant technical changes from the previous edition (EIA/JESD61, April 1997) to make it applicable to copper as well as to aluminum metallizations. Substantive changes to the document are listed in Annex D.

Introduction

As the copper damascene technology has gained widespread use for ULSI interconnections, a renewed interest has developed in fast wafer level reliability (WLR) measurements to evaluate electromigration. The standard package level reliability (PLR) tests, used in the semiconductor industry, are very expensive when applied to copper metallizations, in comparison with aluminum-based structures, due to the considerable cost of the high temperature environmental chambers required (a typical stress temperature is 350 °C) and to the time (weeks, months) required to perform some characterizations.

Standardized WLR methods, as the Isothermal Test (JESD61) [1], [2], [3], [4], the Standard Wafer level Electromigration Accelerated Test (JEP119A) [5], and the Constant Current Test (JESD202) have been applied to the evaluation of electromigration in copper, with the aim not to substitute for PLR tests, rather to provide a less expensive tool to complement them: only a wafer prober and some relatively inexpensive measurement instruments are needed. The speed of WLR measurements is a key issue in the production line to monitor and give feedback on the quality of the metallization.

In this scenario it is fundamental to achieve the best correlation between the PLR and WLR tests [6], [7]. The isothermal test has been cited as being the most suitable method [8]: a constant and uniform temperature is assumed in the test line, close to the situation achieved in the moderately accelerated constant-current PLR tests.

Introduction (cont'd)

In fact, the assumption of a uniform temperature in the line during the isothermal test can be a poor approximation unless appropriate thermal modeling and test structure designs are used to minimize the unavoidable temperature gradients at the line ends. Hence, when meaningful correlations between PLR and WLR tests results are desired, such efforts are very important.

Moreover, it is necessary to enhance the temperature accuracy on copper structures, where temperatures as high as 600 °C can be reached during WLR tests. The present revision JESD61A introduces the recommendations for a correct temperature determination [5], [9], [10], previously incorporated in JEP119A (Procedure for SWEAT) and in JESD33B (Standard for TCR measurement).

ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE

1 Scope

This document describes a procedure for conducting the ISOthermal accelerated wafer level electromigration Test (ISOT) [1], [2], [3], [4] using computer-controlled instrumentation. This procedure is suitable for aluminum as well as for copper metallizations. There is no limitation to the use of this procedure at lower acceleration levels, down to and including the levels used for the conventional PLR electromigration test.

This document does not specify what test structure to use with this procedure. A standard describing the design features to be adopted to minimize the temperature gradients (see 7.5) in highly-accelerated WLR measurements is not presently available. However, users of this procedure report its effectiveness with both straight-lines and via-terminated test structures.

2 Normative references

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revision of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative references indicated below. For undated references, the latest edition of the normative document referred to applies.

JEDEC JESD33B, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line*, February 2004.

JEDEC JEP119A, *A Procedure for Performing SWEAT*, August 2003.

ASTM F 1259M-96, *Standard Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Due to Electromigration*, Reapproved 2003.

JEDEC JESD87, *Standard Test Structures for Reliability Assessment of AlCu Metallizations with Barrier Materials*, July 2001.

JEDEC JESD37, *Standard for Lognormal Analysis of Uncensored Data, and of Singly Right-Censored Data Utilizing the Persson and Rootzen Method*, October 1992.

JEDEC JESD202, *Method for Characterizing the Electromigration Failure Time Distribution of Interconnect Under Constant-Current and Temperature Stress*, March 2006.

3 Terms and definitions

For the purposes of this standard, the following terms and definitions apply.

3.1 test structure

A passive metallization structure, including a test line, that is fabricated on a semiconductor wafer by procedures used to manufacture microelectronic integrated devices.

NOTE Connections are provided to make Kelvin-like resistance measurements of the test line, i.e., two taps for sensing voltage when two other terminals force a current through the line. Typically, these terminals are located at the ends of the test line in single-level structures, while multi-level structures have vias that connect the ends of the test line to the over- or underlying metal level in which the terminals are located (see also 7.5).

3.2 test line

A metallization line, of specified dimensions, whose length is defined by the position of the two voltage taps for single-level structures or by the position of the vias for multi-level structures, which locate the taps in a different metal level.

NOTE 1 It is assumed that the major portion of the test-line length will have a uniform cross-sectional area. This supports the assumption of approximately uniform temperature along the length. This statement holds true as long as significant voiding has not occurred. The assumption is not true at the forcing ends, where a temperature gradient will exist and should be minimized by a proper design in order that the test structure can be suitable for isothermal tests (see 7.5).

NOTE 2 The cross-sectional area of the test line may be either the mean geometrical cross-sectional area or the electrical cross-sectional area. The latter is determined by a method (see subclause 6.3.2 of JESD202, [9], [11]) based on the knowledge of the parameter $\Delta\rho/\Delta T$ for a given material, e.g., Al or Cu, where ρ is the resistivity of the pure, bulk form of the metal, and T is the temperature.

3.3 temperature coefficient of resistance [TCR(T_{ref})] {ºC^{-1}}

The fractional change in resistance of the test line per unit change in temperature at a specified temperature, T_{ref}, as described in the following equation:

$$\mathrm{TCR}\left(T_{\mathrm{ref}}\right)=\frac{1}{R\left(T_{\mathrm{ref}}\right)}\times\frac{\Delta R}{\Delta T} \tag{1}$$

where

$R(T_{ref})$ {Ω} is the resistance of the test line at the reference temperature T_{ref} {ºC};

ΔR {Ω} is the change in resistance;

ΔT {ºC} is the change in temperature that caused the change in resistance.

NOTE 1 Two choices of T_{ref} are in common use: 0 °C and ambient temperature (typically from 24 to 27 °C). They are equivalent as long as self-consistent definitions are used. The choice of 0 °C is preferred, since it facilitates a first-glance comparison of interlaboratory experiments and of experiments conducted at different times in the same laboratory.

NOTE 2 For aluminum-based metallizations, the change in resistance of the test line with temperature, $\Delta R/\Delta T$, is approximately constant from room temperature to about 420 °C. For copper-based metallizations, a variation in $\Delta R/\Delta T$ value becomes evident at temperatures as low as 200 °C [9], [10]. Hence, if the TCR is to be used to calculate the temperature of a copper test line at higher temperatures, a correction factor, F_{corr}, will be required (see 6.1.2).

3 Terms and definitions (cont'd)

3.4 thermal resistance (R_{th}) {ºC/W}

The change in mean temperature of the test line divided by the change in power dissipation in the line, as described in the following equation:

$$R_{th} = \Delta T / \Delta P \quad (2)$$

where

ΔT {ºC} is the change in mean temperature;

ΔP {W} is the change in power dissipation that caused the change in mean temperature.

NOTE 1 It is assumed that the electromigration damage, occurred during the isothermal test, does not affect the thermal resistance of the line to the first order.

NOTE 2 The thermal resistance R_{th} is defined under the assumptions of temperature uniformity along the test line and linear dependence of T versus P: in a plot of T versus P, R_{th} is the slope of the straight line. R_{th} is dependent on the geometry of the test structure and on the thermal conductance of the test line to the ambient. On the other hand, because the thermal conductance of the materials in the path of the heat flow from the test structure are temperature dependent [5], [10], the T versus P relationship is not linear, i.e., the slope of this curve will gradually decrease with increasing power dissipation. In other words, R_{th} is temperature dependent. However, over a limited range of temperatures (typically 50 °C), the T versus P relationship can still be considered linear, assuming the relationship[†]

$$T = T_0^* + R_{th}^* \times P \quad (3)$$

As a consequence, a best straight-line fit of eq. (3), using some measured (T, P) data pairs in this limited temperature range, can be used to estimate the thermal resistance value, R_{th}^*, and the thermal resistance intercept value, T_0^* (see 6.1.7, 6.2.3.3).

3.5 target stress temperature (T_{test}) {ºC}

The desired mean temperature of the test line during the stress phase of the test.

3.6 error band (B_E) {ºC}

A band of test-line temperatures centered on T_{test}, i.e.

$$T_{test} - B_E/2 \le T \le T_{test} + B_E/2 \quad (4)$$

where the isothermal algorithm will consider the test-line temperature to be equal to T_{test}, as required during the stress.

NOTE A typical value for B_E is 1 ºC. However, the feedback control loop will continue to adjust the forcing current, to keep a constant target stress temperature, T_{test}, even when the test-line temperature is within the error band (see 6.3.3).

[†] Throughout this document, the quantities thermal resistance R_{th}^* and intercept T_0^* were obtained from a linear fit to eq. (3) and apply only in the limited temperature range (typically 50 °C) within which the fit was performed.

4 Symbols

For the purposes of this standard, the following symbols are used.

A	empirical constant in Black's equation (see 7.6, Annex B)
a	cross-sectional area of the test line
B_E	temperature error band (see 3.6)
D_i	fractional electromigration damage (see Annex B)
D_{st}	total electromigration damage incurred during the initial settling time (see Annex B)
$\Delta R/R\%$	percent failure criterion (see 6.3.4)
$\Delta R/R\%\big\vert_{init}$	percent failure criterion during the initialization phase (see 6.1.6)
$\Delta R/R\%\big\vert_{step}$	percent failure criterion during staircase/convergence phase (see 6.2.4)
E_a	activation energy in Black's equation (see 7.6, Annex B)
F_{corr}, $F_{corr,\,inv}$	correction factors for TCR application at high temperatures (see 6.1.2)
$f_{current}$	initial current multiplication factor (see 6.1.3)
f_{power}	convergence power reduction factor (see 6.2.1, 0)
I	forcing current through the test line
I_G	range of the current generator (see 6.2.2)
$I_{test,1}$	stress current at convergence (see 6.3.1)
I_1	initial forcing current in the test line (see 6.1.3)
$_i$ (subscript)	index in temperature control loops
J	current density in the test line
J_{test}	stress current density (see 6.3.1)
$J_{test,\,av}$	average stress current density in a sample population (see 7.6)
k	Boltzmann's constant
N_{conv}, $N_{staircase}$	number of temperature steps in convergence, staircase phases (see 6.2.3, Annex A)
$_n$ (subscript)	index in temperature control loops
n	current density exponent in Black's equation (see 7.6, Annex B)
P	power dissipated across the voltage taps of the test line
P_{test}	power at target stress temperature (see 6.3.1)
R	resistance of the test line
R_{end}	resistance value after the isothermal test
R_{fail}	failure resistance value (see 6.3.4)
$R_{fail,\,init}$	failure resistance value during the initialization phase (see 6.1.6)
$R_{fail,\,step}$	failure resistance value during the staircase/convergence phase (see 6.2.4)
$R_{test,1}$	resistance value at convergence
R_{th}	thermal resistance of the test line (see 3.4)
R_{th}^*	R_{th} value, estimated over a limited temperature range (see 3.4, 6.1.7, 6.2.3.3)

4 Symbols (cont'd)

$R^*_{\text{th, test}}$	R_{th} value at convergence (see 6.3.1)
ρ	resistivity of the bulk pure form of the test-line metal
T	mean temperature of the test line
T_{cal}	test-line temperature estimated by TCR, without correction (see 6.1.2)
T_{chuck}	chuck (or ambient) temperature (see 7.1)
T_{conv}	starting convergence temperature value (see Annex A)
TCR	Temperature Coefficient of Resistance (see 3.3)
T_{ref}	reference temperature for TCR (see 3.3)
$T_{\text{staircase}}$	staircase temperature limit (see 6.2.1)
T_{test}	target stress temperature (see 3.5, 6.3.1, 7.6)
TTF	Time-To-Failure
TTF_{corr}	TTF value corrected to account for the initial EM damage (see 6.4.1, Annex B)
TTF_{norm}	TTF value normalized versus the average stress current density $J_{\text{test,av}}$ (see 7.6)
T^*_0	R_{th} intercept value, estimated over a limited temperature range (see 3.4, 6.1.7, 6.2.3.3)
$T^*_{0,\text{ test}}$	R_{th} intercept value at convergence (see 6.3.1)
t	elapsed time for isothermal test after I_1 is applied (see 6.1.3)
t_{corr}	Time-To-Failure correction time (see 6.4.1, Annex B)
t_{log}	time interval for data logging during the stress phase (see 6.4.4)
t_{st}	initial settling time (see 6.4.1, Annex B)
t_{50}	median time-to-failure calculated by Black's equation (see 7.6)
V_{C}	voltage range of voltmeter and compliance of the current generator (see 6.1.5, 6.2.2)
V_{meas}	voltage measured across the voltage taps of the test line (see 6.1.4, 6.2.3, 6.3.3)

NOTE Throughout this document, the bar over symbols will indicate the predicted values when should be distinguished from the measured values (indicated by symbols without bar).

5 Technical requirements

5.1 Equipment requirements

a) A programmable current source capable of supplying sufficient current to attain the required current densities in the metallization test line. Typically, a current density of 1×10^8 A/cm^2 is sufficient. The voltage compliance of the current source shall be sufficient to allow stressing test lines in the resistance range of interest (typically a few Ω to several kΩ). Minimum forcing current resolution of 12 bits, or 3½ digits, is recommended. The current source settling time (i.e. the time required to deliver 99% of the target current) shall be no greater than 10 ms.

b) A digital voltmeter capable of measuring the expected voltages. Three or more full scale ranges may be required (e.g. 1, 10 & 100 V). Minimum measurement resolution of 12 bits, or 3½ digits, is required. Voltmeter conversion time shall be no greater than 10 ms (for additional considerations on voltmeter integration time and input filter see 7.3 and 7.4).

c) A computer acting as a controller. The computer provides a feedback control system. It controls the input current to the metallization under test based on discrete time measurements provided by the voltmeter and computations supervised by the isothermal test algorithm.

The data acquisition time for the feedback control shall be no shorter than the sum of the settling time of the current source and the reading rate of the voltmeter. However, a control cycle time shorter than 50 ms is not recommended (see 7.4 for additional comments).

Time-to-failure (TTF) targets can range from tens of seconds to tens of thousands of seconds. The system should be capable of executing one control cycle with a period short enough to provide a resolution of at least 1% of the TTF.

5.2 Test configuration

Due to the required accuracy for the resistance measurements, a four-wire Kelvin connection to the structure is required. Depending on the test line and stress conditions, a relatively high current may need to be applied. The current-forcing connections to the test structure must be able to sustain this current.

6 The isothermal test algorithm

The isothermal test [1], [2], [3], [4] uses a feedback control loop to adjust the stress current applied to the metallization such that the mean temperature of the test line is maintained within a programmed error band B_E centered around the target stress temperature T_{test}.

The ISOT algorithm is based on a very simple thermal model for the structure. The model assumes linear heat flow from the structure in one dimension based on uniform power dissipation along the length of the structure. It does not consider thermal conduction through the ends to the pads, or temperature gradients in the test line (see 7.5). It is assumed also that the change in resistance of the test line due to electromigration damage does not, to a first-order approximation, affect its thermal resistance. The Temperature Coefficient of Resistance of the test line (see 3.3) must have been determined prior to the test.

The test procedure consists of five main phases, which are briefly described below and in greater detail in 6.1 to 6.4. Figure 1 illustrates how the temperature of the test line increases with time during the first three phases, called the **initial settling time**, t_{st}, followed by the beginning of the stress phase at constant temperature.

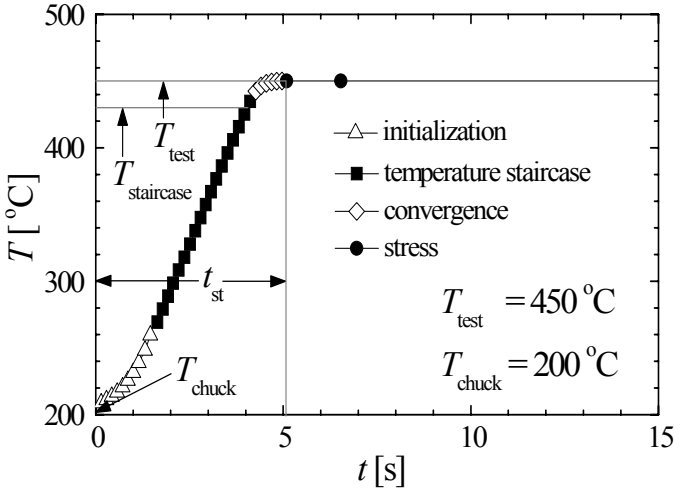

Figure 1 – Measurement phases of the isothermal test

a) **Initialization phase** (see 6.1): Measure the resistance of the test line at the chuck temperature, T_{chuck}, before the test structure is subjected to Joule heating. Apply a suitable current through the test line and, then, measure the resistance as the current is step-wise increased to elevate the test line temperature to 50 °C greater than T_{chuck}. Calculate the initial value for the thermal resistance from the test line temperature data, obtained by the measured resistance data and the TCR, versus applied power data. The time that the current is first applied is the starting time for the isothermal test.

b) **Temperature staircase phase** (see 6.2): Step-wise increase the temperature of the line due to Joule heating, by increasing the applied current. The procedure relies on the balanced use of the TCR, to correlate temperature and resistance of the line, and of the thermal resistance, to estimate the needed current increment. To account for the non-linearity in the temperature versus power relationship, the thermal resistance is recalculated at each temperature step.

6 The isothermal test algorithm (cont'd)

c) **Convergence phase** (see 6.2): Above a given temperature value, $T_{staircase}$, approach smoothly the target stress temperature, T_{test}, to avoid overshoot over the permitted error band.

d) **Stress phase** (see 6.3): Stress at a constant temperature, T_{test}, using the last measured thermal resistance value to regulate the applied current. Only the initial period of this phase is shown in Figure 1.

e) **Exit-at-failure phase** (see 6.4)**:** Halt test when a specified failure criterion is met and estimate the time to failure (TTF). This phase is not shown in Figure 1.

As a first approximation, the TTF is calculated as the time elapsed in the stress phase, i.e. the period between the end of the convergence phase and the occurrence of the failure in the test line (see 6.4.1).

This definition for TTF neglects completely the possibility that electromigration damage occurred during the initial settling time, t_{st}, in particular at the end of the temperature staircase phase and during the convergence phase, when the temperature and the current in the test line are close to the target stress conditions.

A method is presented in Annex B to account for the electromigration damage, incurred during the initial settling time. In this way, it is possible to obtain optionally a corrected value of the TTF by summing to the original value a calculated time, t_{corr}, which accounts for this damage.

Each phase of the isothermal test will be described in detail in the following subclauses.

6.1 Initialization phase

During this phase the line temperature is raised gradually up to 50 °C over the chuck temperature by increasing the current. Then, the initial value of the thermal resistance is calculated through the measured temperature and power data.

The Temperature Coefficient of Resistance, TCR(T_{ref}), of the test line at the reference temperature T_{ref} must have been determined previously, following the procedure in JESD33B (see 7.2 for additional comments).

The initialization phase is illustrated in the flow chart of Figure 2 and the steps take are described in the following subclauses.

6.1.1 Measure the resistance at chuck temperature

For the measurement of the starting resistance of the test line, $R(T_{chuck})$, at the chuck temperature, T_{chuck}, a procedure based on JESD33B should be followed, using a current small enough to cause negligible Joule heating. To avoid errors due to thermal and other emf voltages, the mean of the voltages measured with both current polarities must be used in the resistance determination. This measurement should be done at the highest resolution. Repeated measurements are suggested for improved precision.

Recommendations on the measurement of T_{chuck} are given in 7.1.

6.1 Initialization phase (cont'd)

6.1.2 Convert TCR(T_{ref}) to TCR(T_{chuck})

It is convenient to assume T_{chuck} as the reference temperature in the isothermal test. Convert TCR(T_{ref}) to TCR(T_{chuck}) by using eq. (6) of JESD33B:

$$\mathrm{TCR}\left(T_{\mathrm{chuck}}\right)=\mathrm{TCR}\left(T_{\mathrm{ref}}\right)\Big/\left[1+\mathrm{TCR}\left(T_{\mathrm{ref}}\right)\times\left(T_{\mathrm{chuck}}-T_{\mathrm{ref}}\right)\right] \tag{5}$$

The value TCR(T_{chuck}) is used to calculate the mean temperature T of the test line from the measured resistance $R(T)$ during the initialization phase as well as during the staircase and convergence phases [10].

As in JESD33B, it can be written that

$$T=T_{\mathrm{cal}}\times F_{\mathrm{corr}}\left(T_{\mathrm{cal}}\right) \tag{6}$$

where

$$T_{\mathrm{cal}}=T_{\mathrm{chuck}}+\frac{R(T)-R\left(T_{\mathrm{chuck}}\right)}{R\left(T_{\mathrm{chuck}}\right)\times\mathrm{TCR}\left(T_{\mathrm{chuck}}\right)}. \tag{7}$$

For aluminum test lines, the value of the correction factor is $F_{corr} = 1$ for temperatures from ambient temperature to at least 420 °C. For copper test lines, $F_{corr} = 1$ for $T_{cal} \le 200$ °C, while for $T_{cal} > 200$ °C

$$F_{\mathrm{corr}}\left(T_{\mathrm{cal}}\right)=1.0167-8.39751\cdot10^{-5}\times T_{\mathrm{cal}}-3.74768\cdot10^{-8}\times T_{\mathrm{cal}}^{2}\le1 \tag{8}$$

Conversely, from TCR(T_{chuck}) it is possible to estimate the resistance $\overline{R}(T)$[‡] from the temperature T (see JEP119A) by

$$\overline{R}(T)=R\left(T_{\mathrm{chuck}}\right)\times\left[1+\mathrm{TCR}\left(T_{\mathrm{chuck}}\right)\times\left(T_{\mathrm{cal}}-T_{\mathrm{chuck}}\right)\right] \tag{9}$$

where

$$T_{\mathrm{cal}}=T\Big/F_{\mathrm{corr,\,inv}}\left(T\right). \tag{10}$$

For aluminum test lines, the value of the inverse correction factor is $F_{corr, inv} = 1$ for temperatures from ambient temperature to at least 420 °C. For copper test lines, $F_{corr, inv} = 1$ for $T \le 200$ °C, while for $T > 200$ °C

$$F_{\mathrm{corr,\,inv}}\left(T\right)=1.01535-7.21714\cdot10^{-5}\times T-6.53459\cdot10^{-8}\times T^{2}\le1 \tag{11}$$

6.1.3 Initial current value and current multiplication factor

To estimate the initial value of the thermal resistance, an initial forcing current I_1 and a current multiplication factor $f_{current}$ should be chosen based on experience. What matters most is that the number of steps in the following control loop, 6.1.4, should be at least five (but not much more) to avoid an overlong time for the line temperature to reach or exceed T_{chuck} + 50 °C and to avoid needless stress to the line before the stress phase. In particular, I_1 could have the same value as used in determining TCR, but also a greater value may be used depending on the magnitude of $f_{current}$. A value for the current multiplication factor of between 1.1 and 1.5 is recommended.

The time when the first forcing current, I_1, is applied, is the **origin of the time base** for the isothermal test.

[‡] Throughout this document, the bar over symbols will indicate the predicted values when should be distinguished from the measured values (indicated by symbols without bar).

6.1 Initialization phase (cont'd)

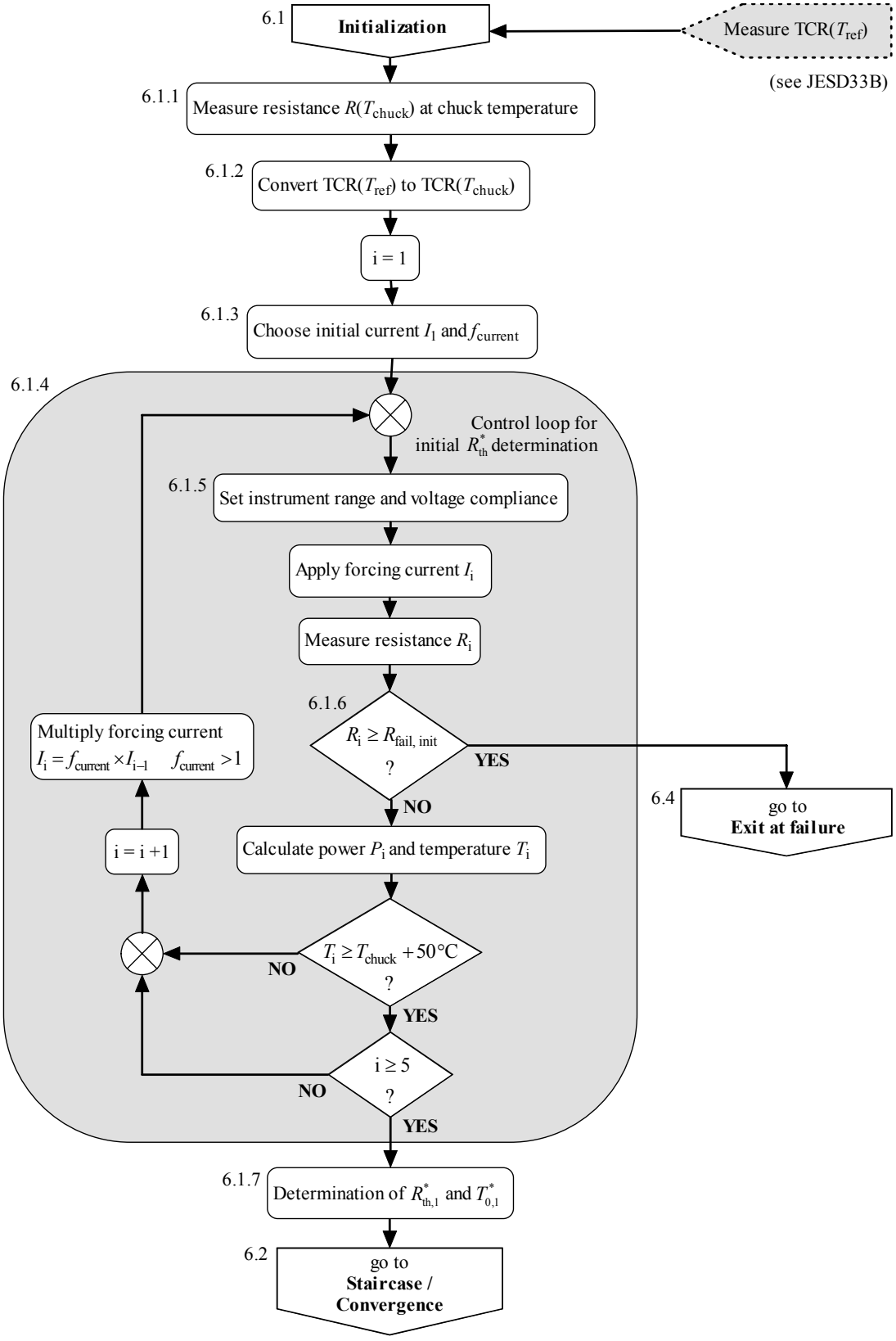

Figure 2 – Flow chart for ISOT initialization phase

6.1 Initialization phase (cont'd)

6.1.4 Control loop to measure the initial thermal resistance

To obtain the initial value for the thermal resistance, perform a control loop (see Figure 2) to increase the forcing current with each iteration (i is indexed):

a) Apply the actual forcing current I_i through the test line. Measure the elapsed time t_i (from the application of the initial forcing current I_1) and store the value for t_i and I_i.

b) Measure the voltage V_{meas} across the voltage taps, compute the resistance $R_i = R(T_i) = V_{meas}/I_i$ and store the value for R_i. Repeated measurements could be employed to assure an improved precision and thermal stability (see 7.3).

c) Calculate the electrical power $P_i = R_i \times I_i^2$ dissipated across the voltage taps, the temperature T_i from R_i, using eqs. (6) and (8), i.e. $T_i = T_{cal,\,i} \times F_{corr}\left(T_{cal,\,i}\right)$ where $T_{cal,\,i} = T_{chuck} + \dfrac{R_i - R(T_{chuck})}{R(T_{chuck}) \times \mathrm{TCR}(T_{chuck})}$, and store the values for T_i and P_i.

d) Exit the control loop if the temperature T_i of the line, increased due to Joule heating, equals or exceeds T_{chuck} + 50 °C and at least five steps have been done, otherwise multiply the forcing current by the factor $f_{current} > 1$, i.e. $I_{i+1} = f_{current} \times I_i$, and iterate this control loop.

The total elapsed time in the initialization phase, from the application of I_1, is defined as the **initialization period**. It is an optionally reported result (see 6.4.3), as well as the values for t_i, I_i, R_i, T_i and P_i at each step, which can be stored in an optional log file (see 6.4.4).

6.1.5 Instrument range and voltage compliance for the initialization phase

The voltage compliance of the current source and the voltmeter range should be set at each step of the ISOT initialization phase to a value

$$V_C > I_i \times \bar{R}\left(T_{chuck} + 50\,^{\circ}\mathrm{C}\right) \tag{12}$$

where the value $\bar{R}\left(T_{chuck} + 50\,^{\circ}\mathrm{C}\right)$ is estimated from eqs. (9), (10) and (11).

6.1.6 Temporary failure criterion for the initialization phase

During the initialization phase a temporary failure criterion is defined, as the maximum percent resistance increment $\Delta R/R\%\big|_{init}$, referred to the maximum predicted resistance $\bar{R}\left(T_{chuck} + 50\,^{\circ}\mathrm{C}\right)$ that is calculated from eqs. (9), (10) and (11), at or above which the structure is considered to have failed. In practice, the test line fails during the initialization phase when the actual value of its resistance equals or exceeds the value

$$R_{fail,\,init} = \bar{R}\left(T_{chuck} + 50\,^{\circ}\mathrm{C}\right) \times \left(100 + \frac{\Delta R}{R}\%\Big|_{init}\right) \Big/ 100 \tag{13}$$

A recommended value for the initialization failure criterion is $\Delta R/R\%\big|_{init} = 100\,\%$.

6.1 Initialization phase (cont'd)

6.1.7 Determination of the initial thermal resistance

In the limited temperature range (50 °C above T_{chuck}) spanned during the initialization phase, the approximate linear relationship (3) between T and P can be written

$$T = T^*_{0,1} + R^*_{th,1} \times P \tag{14}$$

and used to estimate the initial values of the thermal resistance, $R^*_{th,1}$, as well as of the thermal resistance intercept $T^*_{0,1} \sim T_{chuck}$ [5], [10].

To obtain these values, perform a best straight-line fit of the T_i versus P_i data pairs (at least five), measured in the range $T_{chuck} \le T \le T_{chuck} + 50\ °C$ and previously stored (see 6.1.4). A correlation coefficient greater than 0.999 is needed to assure that the dependence of temperature on power is sufficiently linear.

6.2 Temperature staircase and convergence phases

These two phases are strictly interlaced, as can be seen in the flow chart of Figure 3. The algorithms used differ in only a few statements.

During these phases, the temperature of the sample, T_n, is gradually increased towards the target stress temperature, T_{test}. A control loop is performed, where at each step the power dissipation is increased by an amount that is based on an iterative recalculation of the thermal resistance (see 6.2.3.3), which can be considered constant in the limited temperature range $T_n - 50\ °C \le T \le T_n$. By this way it is possible to obtain a gradual temperature rise that is continuous from the preceding to the following ISOT phases [3]. Moreover, this method is not burdensome for the control computer, because it exploits the same best straight-line fit routine which estimates the initial thermal resistance.

In the temperature staircase phase, a fixed temperature step, ΔT, is imposed (see 6.2.1) so that the temperature increases in a constant-slope-staircase fashion (see 0). This phase ends when the temperature of the test line, T_n, is sufficiently close to T_{test} to require a smoother approach to T_{test}.

In the subsequent convergence phase, a decreasing, variable temperature increment is used (see 0) to avoid an overshoot of the line temperature out of the permitted error band. At each step, the sample is supplied only with a fraction of the power needed to reach the upper bound of the error band, i.e. $T_{test} + B_E/2$, but this phase ends when the line temperature reaches or exceeds T_{test}, the target stress temperature (see Annex A for details).

Some criteria should be defined (see 6.2.4) to check for failure before the staircase/convergence phases come to an end, and for any irregular temperature step in the same phases.

6.2 Temperature staircase and convergence phases (cont'd)

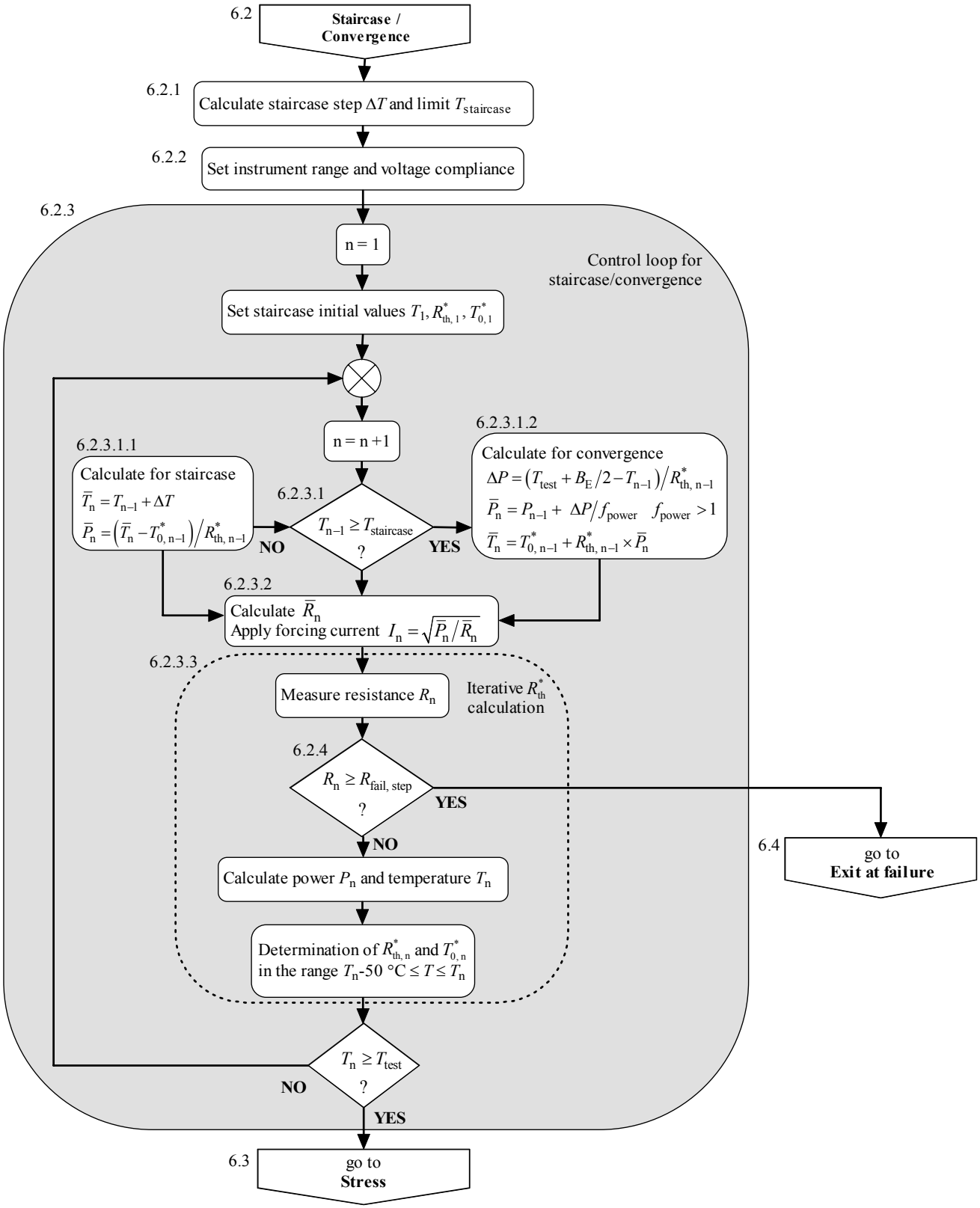

Figure 3 – Flow chart for ISOT temperature staircase and convergence phases

6.2 Temperature staircase and convergence phases (cont'd)

6.2.1 Calculate the temperature step and the staircase temperature limit

The temperature increment for each step, ΔT, must be chosen in order to make the recalculation of the thermal resistance feasible by a linear fit on at least five points [P, $T(P)$] in a 50 °C range. Therefore, it shall be chosen so that $\Delta T \le 10\,°\mathrm{C}$.

The staircase phase, starting from the temperature reached in the preceding phase (approximately T_{chuck} + 50 °C) ends when the actual temperature T_{n} is close enough to T_{test} so that a smooth convergence to T_{test} can be attained and an overshoot can be avoided. This temperature is called $T_{\mathrm{staircase}}$ (shown in Figure 1) and is given by:

$$T_{\mathrm{staircase}} = T_{\mathrm{test}} - f_{\mathrm{power}} \times \Delta T \tag{15}$$

where the numerical factor $f_{\mathrm{power}} = 2$ is defined in the following convergence phase (see 0).

6.2.2 Instrument range and voltage compliance for staircase/convergence/stress phases

Calculate instrument settings suitable for the staircase and for the convergence phases, as well as for the stress phase as follows. Estimate the power at the target stress temperature $\overline{P}_{\mathrm{test}} = \left(T_{\mathrm{test}} - T^{*}_{0,1}\right) \Big/ R^{*}_{\mathrm{th},1}$ from eq. (14). Estimate, from eqs. (9), (10) and (11), the line resistance at the target stress temperature, before any electromigration damage

$$\overline{R}\left(T_{\mathrm{test}}\right) = R\left(T_{\mathrm{chuck}}\right) \times \left[1 + \mathrm{TCR}\left(T_{\mathrm{chuck}}\right) \times \left(T_{\mathrm{test}} \Big/ F_{\mathrm{corr,\,inv}}\left(T_{\mathrm{test}}\right) - T_{\mathrm{chuck}}\right)\right] \tag{16}$$

Set the current source range to a value

$$I_{\mathrm{G}} > \sqrt{\overline{P}_{\mathrm{test}} \Big/ \overline{R}\left(T_{\mathrm{test}}\right)} \tag{17}$$

as well as the voltage compliance of the current source and the voltmeter range to a value

$$V_{\mathrm{C}} > \sqrt{\overline{P}_{\mathrm{test}} \times \overline{R}\left(T_{\mathrm{test}}\right)} \tag{18}$$

6.2.3 Control loop for the temperature staircase and convergence phases

From the values obtained at the end of the initialization phase, at the last i-iteration of the control loop 6.1.4, set the initial values of the temperature and of the thermal resistance in the staircase phase.

Then, starting from the temperature of $T_1 \sim T_{\mathrm{chuck}} + 50\,°\mathrm{C}$, reached at the end of the initialization phase, perform at each iteration of the staircase/convergence control loop (n is indexed) the actions described in the following subclauses, to increase the temperature towards T_{test} (see Figure 3).

The algorithm switches (see 6.2.3.1) from a fixed temperature step ΔT (temperature staircase phase) to a variable temperature step (convergence phase) when the temperature value $T_{\mathrm{staircase}}$ (see eq. (15)) is reached or exceeded during the control loop.

Finally, the control loop ends when the line temperature reaches or exceeds the target stress temperature T_{test} (but the temperature is still included in the error band, see 3.6, Annex A). At this point, the subsequent stress phase will begin (see 6.3).

6.2 Temperature staircase and convergence phases (cont'd)

6.2.3 Control loop for the temperature staircase and convergence phases (cont'd)

The number of iterations in the temperature staircase phase is approximately

$$N_{\text{staircase}} \approx \frac{T_{\text{staircase}} - \left(T_{\text{chuck}} + 50\,^{\circ}\text{C}\right)}{\Delta T} \tag{19}$$

where the total elapsed time in the staircase phase is approximately the acquisition time of the test line resistance value (see 7.3) multiplied by $N_{\text{staircase}}$. This **temperature staircase period** is an optionally reported result (see 6.4.3).

The duration of the convergence phase is approximately equal to the acquisition time (see 7.3) multiplied by the number of iterations N_{conv} in the convergence phase. In turn, N_{conv} depends on both ΔT and the f_{power} factor (see 0), as well as on the temperature reached at the end of the staircase phase. More details are given in Annex A. The **convergence period** is also an optionally reported result (see 6.4.3).

At each step of the control loop, the measurement data (i.e. elapsed time, current, temperature, power, resistance) can be stored in an optional log file (see 6.4.4).

6.2.3.1 Iterative power calculation

In Figure 3, a decision box differentiates the calculation of the needed power between the temperature staircase and the convergence phases, checking if the temperature measured in the previous step, $T_{\text{n-1}}$, has reached or exceeded $T_{\text{staircase}}$ or not.

Iterative power calculation for the temperature staircase phase

In the staircase phase ($T_{\text{n}-1} < T_{\text{staircase}}$) the power is calculated to increase the temperature by the fixed temperature step ΔT.

a) Estimate the temperature at the next step $\overline{T}_{\text{n}} = T_{\text{n}-1} + \Delta T$.

b) Estimate the electrical power

$$\overline{P}_{\text{n}} = \left(\overline{T}_{\text{n}} - T^{*}_{0,\,\text{n}-1}\right) \Big/ R^{*}_{\text{th},\,\text{n}-1} \tag{20}$$

necessary to reach $\overline{T}_{\text{n}}$, using the values of the thermal resistance $R^{*}_{\text{th},\,\text{n}-1}$ and intercept $T^{*}_{0,\,\text{n}-1}$ that were determined in the previous iteration, see eq. (24). Use as initial $R^{*}_{\text{th},\,1}$ and $T^{*}_{0,\,1}$ values those calculated in 6.1.7.

6.2.3 Control loop for the temperature staircase and convergence phases (cont'd)

6.2.3.1 Iterative power calculation (cont'd)

Iterative power calculation for the convergence phase

In the convergence phase ($T_{n-1} \geq T_{staircase}$) the power is calculated by using the values of the thermal resistance $R^*_{th,\,n-1}$ and thermal resistance intercept $T^*_{0,\,n-1}$ that were determined in the previous iteration, see eq. (24).

a) Estimate the new power to be applied

$$\overline{P}_n = \Delta P / f_{power} + P_{n-1} \tag{21}$$

where

$$\Delta P = \left(T_{test} + B_E/2 - T_{n-1}\right) / R^*_{th,\,n-1} \tag{22}$$

is the power increment that is necessary to reach the upper bound of the error band, $T_{test} + B_E/2$. In eq. (21), ΔP is reduced by the convergence power factor $f_{power} = 2$ to avoid overshoot (see Annex A for more details on the convergence algorithm).

b) Calculate the new predicted temperature,

$$\overline{T}_n = T^*_{0,\,n-1} + R^*_{th,\,n-1} \times \overline{P}_n \,. \tag{23}$$

6.2.3.2 Iterative forcing current calculation

c) Estimate the resistance $\overline{R}_n = \overline{R}\left(\overline{T}_n\right) = R\left(T_{chuck}\right) \times \left[1 + TCR\left(T_{chuck}\right) \times \left(\overline{T}_n / F_{corr,\,inv}\left(\overline{T}_n\right) - T_{chuck}\right)\right]$ of the test line at the predicted temperature $\overline{T}_n$, using eqs. (9), (10) and (11).

d) Calculate the new forcing current $I_n = \sqrt{\overline{P}_n / \overline{R}_n}$, which is needed to heat the line to the predicted temperature, $\overline{T}_n$. Apply I_n through the test line. Measure the elapsed time t_n (from the application of the initial forcing current I_1) and store the value for t_n and I_n.

6.2 Temperature staircase and convergence phases (cont'd)

6.2.3 Control loop for the temperature staircase and convergence phases (cont'd)

6.2.3.3 Iterative thermal resistance calculation

e) Measure the voltage V_{meas} across the voltage taps, compute the resistance $R_{\text{n}} = R\left(T_{\text{n}}\right) = V_{\text{meas}} / I_{\text{n}}$ and store the value R_{n}. Repeated measurements could be employed to assure an improved precision and the thermal stability (see 7.3).

f) Calculate the electrical power $P_{\text{n}} = R_{\text{n}} \times I_{\text{n}}^2$ dissipated across the voltage taps, and the temperature T_{n} from R_{n}, using eqs. (6) and (8), i.e. $T_{\text{n}} = T_{\text{cal, n}} \times F_{\text{corr}}\left(T_{\text{cal, n}}\right)$, where

$T_{\text{cal, n}} = T_{\text{chuck}} + \dfrac{R_{\text{n}} - R\left(T_{\text{chuck}}\right)}{R\left(T_{\text{chuck}}\right) \times \text{TCR}\left(T_{\text{chuck}}\right)}$. Store the values for T_{n} and P_{n}.

g) As in the initialization phase (see 6.1.7), a linear relationship (see eq. (3)) between T and P can be assumed in a limited temperature range (50 °C below T_{n}) and written as

$$T = T_{0,\text{n}}^{*} + R_{\text{th, n}}^{*} \times P \tag{24}$$

To obtain the new value for the thermal resistance $R_{\text{th, n}}^{*}$ as well as the intercept $T_{0,\text{n}}^{*}$, perform a best straight-line fit of the T_{n} versus P_{n} data pairs (at least five), measured in the range $T_{\text{n}} - 50\,°\text{C} \le T \le T_{\text{n}}$ and previously stored. A correlation coefficient greater than 0.999 is needed to assure that the dependence of temperature on power is sufficiently linear. In the initial steps of the temperature staircase phase, the [P, $T(P)$] data pairs stored for the determination of initial thermal resistance (see 6.1.4) will have to be used until 50 °C have been spanned in the staircase phase.

6.2.4 Temporary failure criteria for staircase and convergence phases

During the staircase and convergence phases, a temporary failure criterion is defined, as the maximum percent resistance increment $\Delta R/R\%\big|_{\text{step}}$, referred to the predicted value of resistance at the target stress temperature $\overline{R}\left(T_{\text{test}}\right)$ that is calculated from eq. (16). In practice, the test line fails, during the staircase/convergence phase, when the actual value of its resistance equals or exceeds the value

$$R_{\text{fail, step}} = \overline{R}\left(T_{\text{test}}\right) \times \left(100 + \frac{\Delta R}{R}\%\Big|_{\text{step}} \right) \Big/ 100 \tag{25}$$

A recommended value for the staircase/convergence failure criterion is $\Delta R/R\%\big|_{\text{step}} = 20\,\%$.

As an option, a criterion could also be introduced to check for an irregular temperature increment, based on the absolute value of the difference between the measured resistance value R_{n} and the predicted value $\overline{R}_{\text{n}}$, divided by the lesser of these two values. This criterion could trigger a WARNING or EXIT condition when the actual percent variation exceeds a stated limit $\Delta R/R\%\big|_{\text{n}}$, i.e.

$$\frac{\left|R_{\text{n}} - \overline{R}_{\text{n}}\right|}{\text{MIN}\left\{R_{\text{n}}; \overline{R}_{\text{n}}\right\}} \times 100 \ge \frac{\Delta R}{R}\%\Big|_{\text{n}} \tag{26}$$

A recommended value for the irregular step criterion is $\Delta R/R\%\big|_{\text{n}} = 20\,\%$.

6.3 Stress phase

The isothermal procedure assumes that the electromigration damage, which causes the change in test-line resistance, does not, to a first-order approximation, affect the test-line thermal resistance, i.e. there is a negligible change in the overall geometry of the line and of its heat dissipation properties. As a consequence, a constant thermal resistance implies a constant power dissipation to maintain a constant mean temperature in the test line, when the chuck temperature is constant (see eq. (2)).

Once the target temperature T_{test} is reached or exceeded in the previous convergence phase (but the temperature is still included in the error band, see 3.6, Annex A) the stress phase begins, where the algorithm switches to the control of the power input to the structure as the best method to maintain a constant effective temperature. In practice, to keep constant the power dissipation $P = R(T_{test}) \times I^2$ in the test line (hence a constant temperature, T_{test}) during the stress phase, perform a control loop (see the flow chart of Figure 4) where the value of the applied current is adjusted downward or upward, depending on the measured line resistance, $R(T_{test})$, which changes due to the electromigration damage.

The stress phase ends when a given failure criterion is reached (see 6.3.4).

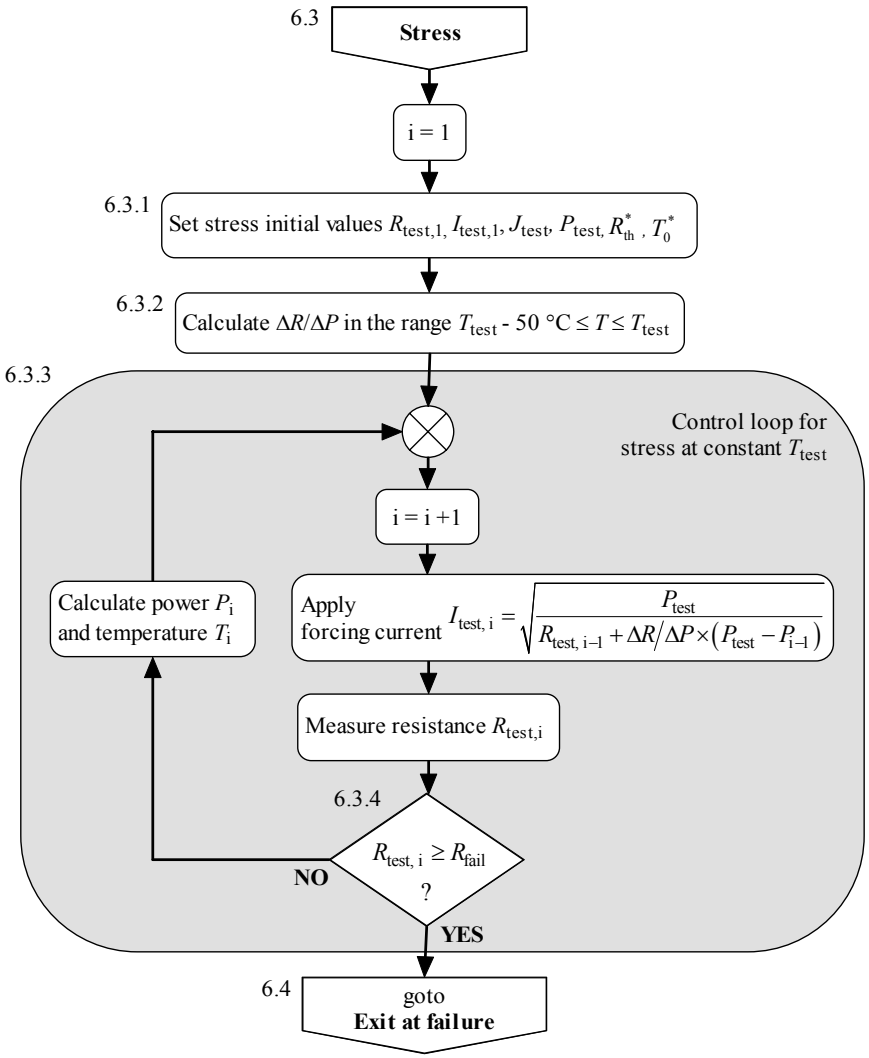

Figure 4 – Flow chart for ISOT stress phase

6.3 Stress phase (cont'd)

6.3.1 Set the power and the initial current at target stress temperature

At the end of the convergence phase, the test line temperature can be considered equal to the target stress temperature T_{test} (see the error band definition 3.6). As a consequence, set the initial values of the stress phase from the values obtained in the last n-iteration of the control loop 6.2.3, as follows:

- The **resistance at convergence** $R_{test,1} = R_n$, which is the initial test line resistance under stress at T_{test}, before any changes due to electromigration damage;
- The **stress current at convergence** $I_{test,1} = I_n$, which is the initial stress current flowing through the line at T_{test}, before any changes due to electromigration damage;
- The **stress current density** $J_{test} = I_{test,1} / a$, where a is the cross-sectional area of the test line;
- The **power at target stress temperature** $P_{test} = P_n = R_{test,1} \times I_{test,1}^2$, to be kept constant during the stress phase to achieve a constant mean temperature T_{test} in the test line, assuming an unvarying thermal resistance (see 3.4);
- The **thermal resistance at convergence** $R^*_{th,\,test} = R^*_{th,\,n}$ as well as the intercept $T^*_{0,\,test} = T^*_{0,\,n}$ are both assumed constant during the stress phase of the test.

6.3.2 Calculate the dependence of the resistance on the effective applied power

A linear, first-order dependence of the test line resistance on the effective applied power is assumed in a limited temperature range around T_{test} [4]. The following relationship will be used to predict the value of the resistance, $\overline{R}_{test,\,i}$, when a power P_{test} is dissipated in the i-iteration of the following control loop 6.3.3, starting from the values of resistance and power, $R_{test,\,i-1}$ and P_{i-1}, measured previously in the (i-1)-iteration

$$\overline{R}_{test,\,i} = R_{test,\,i-1} + \frac{\Delta R}{\Delta P} \times \left(P_{test} - P_{i-1} \right) \tag{27}$$

The value of $\Delta R / \Delta P$ is estimated from a best straight-line fit of the R_n versus P_n data pairs (at least five), measured and stored in the range $T_{test} - 50\ °C \le T \le T_{test}$ during the staircase/convergence phases (see 6.2.3.3). A correlation coefficient greater than 0.999 is recommended to assure the linearity of the relationship.

6.3.3 Control loop to maintain a constant stress temperature

Perform a feedback control loop (see Figure 4), where at each iteration (i is indexed):

a) Calculate the next value of the forcing current

$$I_{test,\,i} = \sqrt{P_{test} / \overline{R}_{test,\,i}} \tag{28}$$

where $\overline{R}_{test,\,i}$ is the next, predicted value for the resistance at P_{test}, calculated from eq. (27). Apply $I_{test,i}$ through the test line. Measure the elapsed time t_i (from the application of the initial forcing current I_1) and store temporarily the values for t_i and $I_{test,\,i}$.

NOTE 1 To a first-order approximation, eq. (28) accounts for the temperature change of the resistance to the predicted value $\overline{R}_{test,\,i}$ when the new value of the current $I_{test,\,i}$ is applied. This predictive feedback algorithm is effective to maintain a constant stress temperature, minimizing possible temperature oscillations in presence of sudden variations of the test line resistance [4].

6.3 Stress phase (cont'd)

6.3.3 Control loop to maintain a constant stress temperature (cont'd)

b) Measure the voltage V_{meas} across the voltage taps, compute the resistance $R_{test,\,i} = R(T_i) = V_{meas} / I_{test,\,i}$ and temporarily store the value for $R_{test,\,i}$.

c) Calculate the actual applied power $P_i = R_{test,\,i} \times I^2_{test,\,i}$.

d) Calculate the actual temperature $T_i = T^*_{0,\,test} + R^*_{th,\,test} \times P_i$, temporarily store the values for T_i and P_i.

NOTE 2 During the stress phase, it is unwise to continue using the TCR method (see 6.1.2) to estimate the test line temperature. In fact, the TCR of the test line could change, due to the electromigration damage (void growth). The test line is better estimated by means of the thermal resistance, which is independent of the damage to the first order [10].

The measured temperature, T_i, could show oscillations out of the chosen error band $T_{test} \pm B_E/2$, because of the feedback response to fast glitches in the measured resistance [4]: in this case, a WARNING condition should be indicated. To reduce oscillations, the feedback cycle time (i.e. the duration of one iteration) shall be not less than 50 ms, as suggested in 7.4 together some other precautions.

For a documentation of the test, the measurement data acquired during the stress phase could be stored permanently in an optional log file, but at a stated interval t_{log} instead of at each iteration, to reduce the memory requirements (see 6.4.4). The data log file could be useful also to diagnose problems in the stress phase, like resistance fluctuations and/or temperature oscillations out of the error band.

6.3.4 Failure criterion for the stress phase

During the stress phase, the failure criterion is defined as the maximum percent resistance increment, $\Delta R/R\%$, referred to the resistance at convergence $R_{test,\,1}$ (see 6.3.1), at or above which the structure is considered to have failed. In practice, the test line fails, during the stress phase, when the actual value of its resistance, $R_{test,\,i}$, equals or exceeds the value R_{fail} defined by

$$R_{fail} = R_{test,\,1} \times \left(100 + \frac{\Delta R}{R}\% \right) \Big/ 100 \tag{29}$$

NOTE 1 In general, the isothermal test is terminated (EXIT condition) when the stress failure criterion is reached, but it could be useful to define a dual criterion, i.e. using an ISOT failure criterion of, e.g., $\Delta R/R\% = 2\%$, but continuing the stress up to a greater variation $\Delta R/R\% = 10\%$, as common in PLR tests [12]. The obvious drawback of the dual criterion is the failure analysis will reflect the damage after the worst failure criterion is reached. In fact, the damage evolution in isothermal tests after a few percent of resistance change is very fast and a catastrophic damage could occur before the test is terminated.

NOTE 2 In some experiments, the additional definition of an absolute failure criterion for a fixed resistance increase may be advisable. For example, during the tests on multilevel structures, often a step resistance increase is observed when metal depletion happens at one via. This kind of failure can be distinguished from the failure due to void formation along the line: in the latter case the electromigration damage produces usually a more gradual resistance increase.

6.4 Exit at failure of the test line

On exiting (see the flow chart of Figure 5), turn off the current so the line temperature goes back to T_{chuck}. Then, supply the same low current used in 6.1.1 to measure $R(T_{chuck})$, and measure, if possible, the resistance $R_{end}(T_{chuck})$ after the test, which is different from the previous value, because of the electromigration damage. Failure conditions must be recorded. In detail, the data to be reported upon exiting the test are described in the following subclauses.

NOTE During each stage of the test, a different failure criterion is established based on the value of the resistance of the test line (see 6.1.6, 6.2.4, 6.3.4). Other EXIT conditions should be allowed for in the algorithm depending on the specific test implementation. These include: short circuit to an extrusion monitor, exceeding current and voltage limits, falling below resolution limits, reaching the maximum number of data points, reaching the maximum test time, stopping the measurement after a WARNING condition, and so forth.

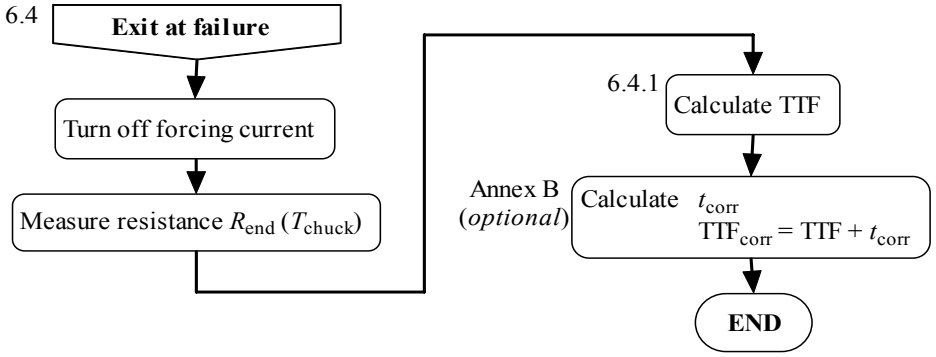

Figure 5 – Flow chart for ISOT exit-at-failure phase

6.4.1 Calculate the time-to-failure (TTF)

When the failure occurred during the stress phase, the measurement data taken in the stress feedback control loop 6.3.3 at the last iteration prior to failure should be considered the final conditions.

As a first approximation, the elapsed time in the stress phase should be considered as the actual **time to failure (TTF)**. It can be calculated as the elapsed time, from the application of the initial forcing current I_1 (see 6.1.3) to the above last iteration, less the initial settling time, t_{st}, i.e. the sum of the initialization, temperature staircase and convergence periods.

Note that this definition for TTF neglects completely the possibility that electromigration damage occurred during the initial settling time, in particular when the temperature and current in the test line are close to the target stress conditions. The influence of this damage can be considered as a function of the TTF: the shorter the failure time, the greater is the impact of the initial settling time on results, or, conversely, the duration of the initial settling time should be negligible with respect to the actual TTF.

In Annex B, a method is presented to estimate the electromigration damage incurred during the initial settling time, t_{st}, which uses the data stored in the optional log file (see 6.4.4). In this way, it is possible to compensate optionally the measured TTF value for having neglected to account for the above damage. This is done by considering an equivalent damage, produced at the target stress conditions (T_{test}, J_{test}) but in a time $t_{corr} < t_{st}$. In practice, the corrected TTF_{corr} can be obtained by summing the calculated t_{corr} with the original TTF value. Just because the damage during the initial settling time can be estimated, there is no justification for increasing the stress conditions to shorten the test time. Using very high stress conditions will induce large thermal gradients that will undermine the validity of test results (see 7.5).

6.4 Exit at failure of the test line (cont'd)

6.4.2 Required data report

- Nominal test line dimensions, cross-sectional area and how determined.
- Temperature coefficient of resistance TCR(T_{ref}) at a reference temperature T_{ref}.
- Target stress temperature T_{test} and error band B_E.
- Percent failure criterion $\Delta R/R\%$.
- Chuck temperature T_{chuck} and initial resistance $R(T_{chuck})$.
- Resistance, $R_{test,1}$, and stress current density, J_{test}, at the end of the convergence phase.
- Time to failure (TTF) and/or indicator of the test phase at the failure.

6.4.3 Optional data report

- Resistance at reference temperature $R(T_{ref})$.
- Value of the low current used to measure $R(T_{chuck})$.
- Value of the initial forcing current, I_1, and current multiplication factor, $f_{current}$.
- Temperature staircase step, ΔT, and convergence power factor, f_{power}.
- Temporary failure criteria (initialization $\Delta R/R\%\big|_{init}$ and staircase/convergence $\Delta R/R\%\big|_{step}$).
- Durations of the initialization, temperature staircase and convergence phases.
- Thermal resistance, $R^*_{th,\,test}$, and intercept, $T^*_{0,\,test}$, at the end of the convergence phase.
- Resistance, $R_{end}(T_{chuck})$, at chuck temperature after the test, or line status (i.e. short, open).

6.4.4 Optional log file

To keep an optional complete log of the test, it is recommended to store a data record for each iteration of the control loops in the initialization phase (6.1.4) and staircase/convergence phases (6.2.3), while in the stress phase (6.3.3), to reduce the memory requirements, store a data record at t_{log} intervals and at the single feedback iteration just before the failure criterion is reached. The choice of the interval t_{log} (typical value: seconds – tens of seconds) is dependent on the required detail in respect to the expected time to failure, i.e. the number of stored data points from the convergence to the TTF.

NOTE The log file could be useful to diagnose problems in the stress phase, like resistance and/or temperature fluctuations. In this case, it could be useful to write, at time intervals shorter than t_{log}, the data records acquired in a stated period, pre- and post- the event to be logged.

The data record (n is indexed) should contain the values of:

- Elapsed time t_n (from the application of the initial forcing current I_1);
- Phase indicator (i.e. initialization/staircase/convergence/stress);
- Predicted temperature $\overline{T}_n$, power $\overline{P}_n$, and resistance $\overline{R}_n$ (excluding initialization and stress phases);
- Applied forcing current I_n;
- Measured temperature T_n, power P_n, and resistance R_n ($R_{test,\,n}$ during the stress phase);
- Thermal resistance, $R^*_{th,\,n}$, and intercept, $T^*_{0,\,n}$ (excluding initialization and stress phases).

The log file is required when the TTF is corrected for the damage incurred during the initial settling time (see 6.4.1, Annex B).

6.5 Isothermal test characteristics

The typical characteristics of the isothermal electromigration test, to be considered when setting up a measurement system, are described in the following list. Specific values are to be selected by the parties to the test.

Target Stress Temperature (T_{test})

Range: from 150 °C to 400 °C for aluminum test lines;
from 250 °C to 600 °C for copper test lines.

Stress Current Density (J_{test})

Range: from 1×10^6 to 1×10^8 A/cm^2.

It is impossible to choose separately J_{test} from T_{test} in an isothermal test. However, the required current density will depend on a number of considerations, such as the metallization material and its susceptibility to electromigration, the thermal resistance of the line, and the chuck temperature.

Chuck Temperature (T_{chuck})

Shall be constant during the test. It is a controllable parameter when a temperature-controlled chuck is used.

Range: from ambient temperature to 200 °C. For copper test lines, a value inside the linear region of the resistance versus temperature relationship is recommended (see 7.1).

Time To Failure (TTF)

Range: From zero to the maximum value compatible with the environment where the test is performed (e.g. production monitoring, periodic test of metallization quality, etc.).

Samples that fail during the initial settling time could be included in the population as "zero time" failures or could be considered as belonging to a weak population (additional failure analysis is required). Samples which do not fail within the maximum test time should be right-censored when obtaining a lognormal fit of the data (see JESD37).

Feedback Cycle Time

Minimum: 50 ms, or several times greater than the thermal time constant of the test structure, whichever is the larger.

Maximum: 500 ms.

Recommended: 100 ms, employing filtering on the voltmeter input to keep temperature oscillations to a minimum (see 7.4).

Initial Settling Time (t_{st})

It is the sum of the initialization, staircase and convergence periods.

Minimum: Limited only by the speed of the system and the accuracy required (see 7.3).

Maximum: It should be negligible in respect to the duration of the stress phase.

When the last condition is not satisfied, it is suggested to correct the measured TTF (see 6.4.1, Annex B), to account for the electromigration damage produced during the initial settling time.

6.6 Example of isothermal test

An example of isothermal electromigration test is illustrated here. The line under test is fabricated in a 3-level dual-damascene copper process, with length of 800 μm, width of 0.19 μm and cross-sectional area of 3.09×10^{-10} cm^2. The structure resembles a standard straight line (see ASTM F 1259M-96), but with vias to connect the line to the taps, which are on a different metal level. The TCR(T_{ref}) value, at the reference temperature T_{ref} = 0 °C, was 0.002488 °C^{-1}. Table 1 lists the parameters used in the test.

Table 1 – ISOT input parameters for a copper damascene line

Parameter	Name	Value
T_{chuck}	Hot chuck temperature	100 °C
I_1	Initial current	5.0 mA
$f_{current}$	Current multiplication factor	1.1
ΔT	Staircase temperature step	10 °C
f_{power}	Convergence power factor	2.0
T_{test}	Target stress temperature	350 °C
B_E	Error band	1 °C
$\Delta R/R\%$	Percent failure criterion	10 %
t_{log}	Interval to store data during stress	10 s

Figure 6 shows the experimental behavior of the temperature versus the time. The temperature was calculated by using eqs. (6) and (7). The figure shows the different phases of the ISOT procedure, with an emphasis on the initial settling time, i.e. on initialization, staircase and convergence phases:

- Initial R^*_{th} determination, at $T_{chuck} \le T \le T_{chuck} + 50\,°C$. The first point corresponds to the temperature increase over T_{chuck} due to the application of the initial forcing current I_1;
- Temperature staircase, with optimal linearity, at $T_{chuck} + 50\,°C \le T \le T_{test} - f_{power} \times \Delta T$;
- Convergence to T_{test} ;
- Stress at constant T_{test}, which continues until the failure criterion is reached.

Starting the time count when I_1 is applied, the duration of the initial settling time is t_{st} = 5.07 s, while the failure occurred at 700.06 s (not shown in Figure 6, see next Figure 7).

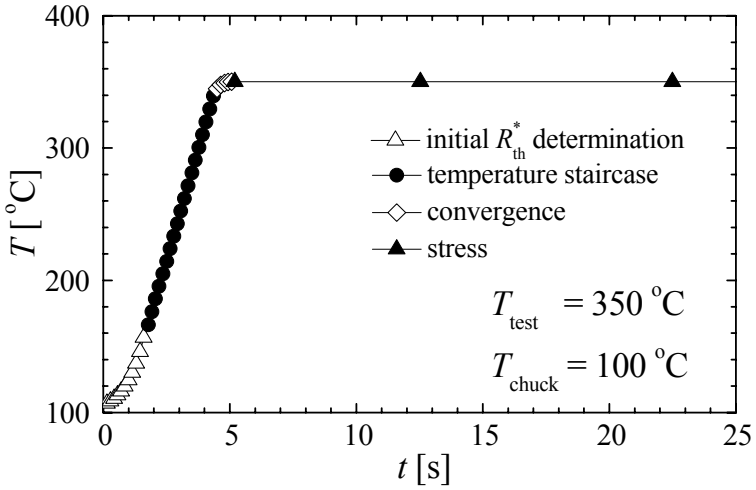

Figure 6 – ISOT temperature behavior

6.6 Example of isothermal test (cont'd)

Figure 7 shows the behavior of the resistance versus the time in a semi logarithmic plot to show the point of failure. The resistance is almost constant throughout the stress phase, till a final increment to the failure value. Note that, during the stress phase, the resistance data were stored at an interval time t_{log} ~ 10 s (see 6.4.4). The test results were: J_{test} = 75.82 MA/cm^2, $R_{test,1}$ = 1153 Ω, TTF = 695 s (the latter is the duration of the stress phase).

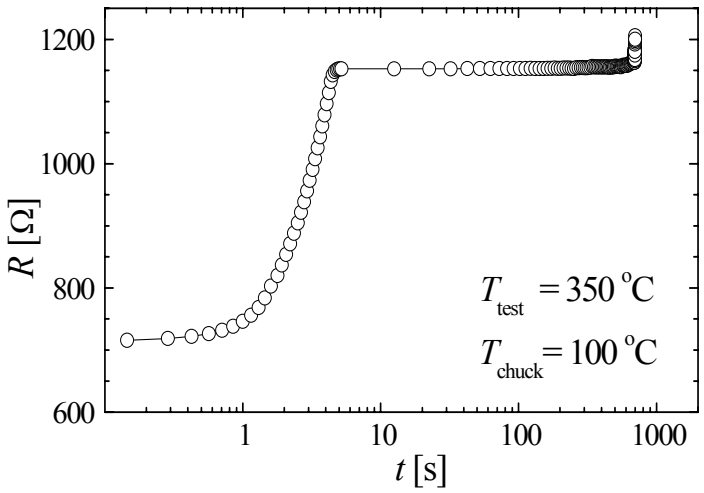

Figure 7 – ISOT resistance behavior

Figure 8 shows the behavior of the thermal resistance R_{th}^* and the intercept T_0^* versus the temperature. The expected decrease of R_{th}^*, when increasing *T*, is clearly visible, due to the increase of the thermal conductivity of the oxide surrounding the test line. Each symbol in the plot represents the result of the best straight-line fit, executed on the [*P*, *T*(*P*)] points measured in a range of 50 °C below the symbol abscissa (see 6.2.3.3). The first points in the plot are at a temperature ~ T_{chuck} + 50 °C (see 6.1.7).

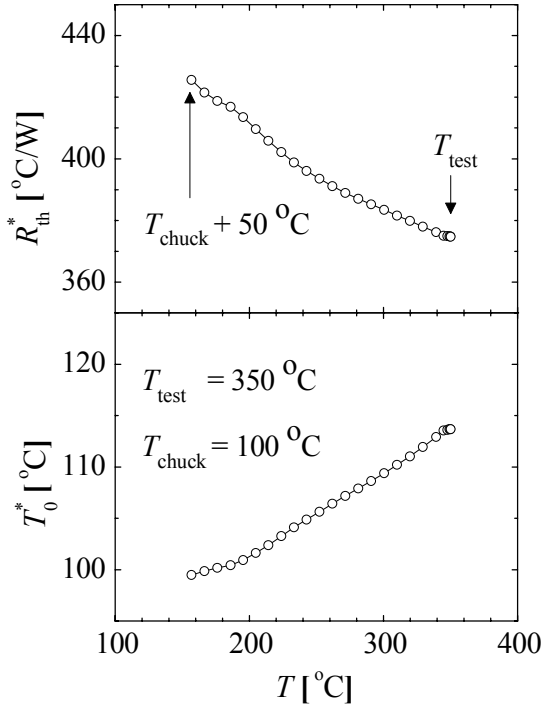

Figure 8 – ISOT thermal resistance behavior

7 Interferences

7.1 Measurement and control of the wafer temperature

In order to measure the temperature of the wafer, T_{chuck}, a temperature sensor in good thermal contact with the chuck shall be used. A temperature display resolution of 0.1 °C and a temperature setpoint accuracy of ± 0.5 °C are suggested.

NOTE 1 As an alternative, should $R(T_{ref})$ of the test line be known, T_{chuck} could be estimated from eq. (1) and the value of $TCR(T_{ref})$

$$T_{chuck} = T_{ref} + \frac{R(T_{chuck}) - R(T_{ref})}{R(T_{ref}) \times TCR(T_{ref})} \tag{30}$$

However, it is recommended that a temperature-controlled wafer chuck or some other means be used to keep constant the temperature of the wafer during the stress tests.

NOTE 2 Keeping constant the temperature of the wafer can avoid several sources for measurement interference that could lead to errors of interpretation in a given test and in tests conducted at different times or in different laboratories. For example: testing many structures over a wafer on a chuck with no temperature control can gradually increase the temperature of the chuck and wafer due to the Joule heating associated with the tests. At the same time, the ambient temperature of the laboratory room could change by as much as several degrees over the period of such tests. Furthermore, the mean and the spread of the ambient temperatures could also differ significantly from one season to the next. The resultant uncertain variability in the ambient temperature of the wafer would be reflected in the stress conditions of the tests and, hence, in the failure times recorded.

The temperature at which the wafer is controlled shall normally be no higher than necessary to maintain a stable temperature of the wafer. This temperature might be the same temperature at which normal parametric tests would be conducted. In any case, if a hot chuck is used, it is recommended to set T_{chuck} to a value inside the linear region of the resistance versus temperature relationship (see 6.1.2). While for aluminum-based metallizations there are no practical limitations (the linear region extends up to 420 °C, far beyond the useful WLR temperature range), for copper-based metallizations $T_{chuck} \leq 200$ °C should be chosen.

NOTE 3 Related to the choice of the chuck temperature, an interesting feature of the isothermal method is the chance to execute more tests, on the same lot, at the same target stress temperature T_{test}, but with different stress current density values, by choosing different values of T_{chuck} [2]. Executing a number of experiments at different conventional stress conditions (see 7.6), it is possible to extract the parameters E_a and n of the Black's equation, which are process dependent.

7.2 Variation in TCR value

The TCR value is dependent on processing through its effect on the residual resistivity of the metallization, which is affected, for example, by impurities, defects, vacancy concentration, grain boundaries, and interfaces [9]. For this reason the TCR may vary from lot to lot, wafer to wafer, or even within wafer. While it may not be practical to measure the TCR for each sample tested, the existence of variation should be recognized as a potential confounding factor. As a minimum, a periodic monitoring of the TCR value for a particular process is recommended on selected lots, preferably using the same structure adopted in the isothermal test.

7 Interferences (cont'd)

7.3 Resistance measurements

To make accurate resistance measurements, the structure must have separate contact pads for forcing current to the test line and sensing voltage (Kelvin connection). Placing two probes on one pad, one to carry current and one to measure voltage, will likely result in unacceptable measurement errors when determining the TCR and the thermal resistance. Less attention needs to be devoted to making accurate measurements during the stress phase of the test because of the relative magnitude of the voltages measured.

Care should be devoted to the endurance of the electrical contacts, as well as to the thermal stability, during the measurement of the line resistance. In fact, the wafer temperature is fixed to the stated chuck temperature, while only the test line reaches the highest temperature, because of the Joule heating in the line. Moreover, the thermal response time of narrow-line test structures due to a forcing current change is very short, less than a few microseconds, but it is necessary to account for the delay needed to program the current source (if not done before), to trigger it and, mainly, to supply the new current value (see 5.1).

NOTE It is suggested that repeated readings be acquired (e.g. at least three) from the voltmeter after a chosen delay (depending on the current source settling time) at a chosen time interval (depending on voltmeter integration time and resolution). Then calculate the average and the standard deviation of these readings, accepting the average as a valid measure when the standard deviation is lower than a chosen percentage (e.g. 1%), otherwise signal a WARNING condition for the contact endurance or for thermal instability. Typically, this procedure is related to the initialization/staircase/convergence phases (6.1.4, 6.2.3.3). During the stress phase (6.3.3), when temperature and resistance are not much variable, the voltmeter delay could be reduced and the acquisition could be simplified (only one reading, without controls) to speed up the feedback control cycle, but care should be taken to reduce possible temperature oscillations due to resistance instability (see 7.4).

7.4 Feedback cycle time

For wafer level testing, the thermal response time of narrow-line test structures due to a current change is less than a few microseconds. Hence, the feedback cycle time is primarily affected by:

- the current source settling time after a requested change in forcing current;
- the voltmeter reading rate (depending on integration time and conversion time);
- the data acquisition and processing times of the controller, which is affected by the instrument interface speed.

The introduction of a substantial delay in the voltage measurement, after a current change has been requested, is not as important during the stress phase because the changes in current in this phase are smaller. Although it may be easy to obtain a feedback cycle time of 20 to 30 ms using modern test equipment with IEEE-488 instrument interfaces, it is recommended that the feedback cycle time should be no less than 50 ms. This recommendation (based primarily on experience) is also given as a means to avoid instability problems, together with the use of a low-pass filter applied to the voltmeter input. In this case the recommended feedback cycle time would increase to about 100 ms.

NOTE Instability phenomena have been observed in the resistance of copper damascene samples during isothermal tests, mainly when approaching failure [4]. In particular, fast and reversible resistance increases have been measured. A cause could be the non-perfect filling of vias and/or conduction through the diffusion barrier, in the presence of large stress-induced voids. While eq. (28) can account for a sudden and afterwards steady resistance step, a fast glitch in the resistance could cause an erroneous measurement. In this case, the feedback control is not effective in keeping the line temperature within $B_E/2$ of T_{test}. To reduce the influence of these glitches, it is suggested to increase the integration time (low-pass input filter) of the voltmeter to 20 or 30 ms.

7 Interferences (cont'd)

7.5 Temperature gradients

Test results and their interpretation can be impacted by anything that promotes non-uniformities in the Joule heating along the test line [13]. Local changes in the design features of the test structure can lead to temperature gradients in the test line. They can be caused, in single-level structures, by changes in line width at the ends of a test line, by varying the cross-sectional area, due to step coverage, and by other localized changes in their thermal resistance to ambient. All these potential problems could be intensified when using multilevel structures with vias [7].

NOTE 1 Presently, a standard is not available to design appropriate test structures for minimizing the temperature gradients in highly-accelerated WLR measurements.

The ASTM standard F 1259M-96 describes single-level, 4-terminal electromigration test structures, which were designed to promote temperature uniformity along the test line [13] in moderately accelerated stress tests. As a consequence, the length of 800 μm was suggested for the test line and the dimensions of the end segments were defined to reduce the temperature gradients at the ends of the line. However, single-level lines feature a large reservoir effect [14] due to the pads, which could abnormally extend the lifetime.

The standard JESD87 describes multi-level, 4-terminal electromigration test structures, but it is presently applied to AlCu metallizations and to PLR tests, where the Joule heating is limited. To be used in isothermal tests, multilevel structures should be designed to minimize the temperature gradients due to the geometric non-uniformity. Via-type test structures are closer to the real lines used in integrated circuits and their reservoir effect can be minimized. Moreover, at equivalent current densities, the TTF of via-type test structures are invariably considerably shorter than those for structures without vias. Hence, to characterize the realistic lifetime of interconnect lines, via-type test structures must be included and so identified (see 5.17 in JESD202).

The temperature gradients impact the accuracy of estimates of the mean stress temperature of the test line and can, if sufficiently large, create unrealistic stress conditions, severe underestimates of the TTF when extrapolated to use conditions, and changes in the location of the failure site. As a consequence, special attention must be paid, when executing ISOT, to avoid excessive stress conditions in the desire to shorten the duration of the test.

NOTE 2 CAD design that simulates the thermal distribution in the line can be useful to minimize temperature gradients. It is suggested also to perform an accurate failure analysis after the WLR characterization to identify weak points in the design, which could cause failures due to localized excessive temperature gradients.

7 Interferences (cont'd)

7.6 Normalization of stress current density

While the isothermal test attempts to maintain a constant effective target stress temperature T_{test}, the stress current density attained, J_{test} (see 6.3), depends on the line resistance and cross-sectional area, the thermal resistance of the line, and, moreover, on the chuck temperature chosen.

When considering an ISOT experiment where similar (i.e. with the same geometry and materials) samples of a lot are stressed at the same T_{test} and T_{chuck}, it is suggested that the average and the standard deviation of the current-density stresses be calculated. The standard deviation is a measure of lot uniformity and the average current density, $J_{test,\,av}$, is used in the following Black's equation [15] to model empirically the **median-time-to-failure** (t_{50}) of this experiment

$$t_{50} = A \times \frac{1}{J_{test,\,av}^{n}} \times \exp\left(\frac{E_a}{k \times \left(T_{test} + 273.16\right)} \right) \tag{31}$$

where:
A is a constant, provided by the user;
n is the current density exponent, provided by the user;
E_a is the activation energy of the dominant damaging process, provided by the user {eV};
k is the Boltzmann's constant ($8.62 \cdot 10^{-5}$ eV/K).

When estimating the t_{50} of this experiment, a straightforward inclusion of the time to failure values, obtained on similar samples of a lot at the same T_{test} and T_{chuck}, may be misleading, without accounting for the different stress current density values, each measured on a particular sample. This difficulty may be circumvented by employing a normalization procedure on the measured TTFs after the experiment is completed.

The normalized TTF_{norm} can be calculated using the expression, derived [16] from Black's equation (31),

$$TTF_{norm} = TTF \times \left(\frac{J_{test}}{J_{test,\,av}} \right)^{n} \tag{32}$$

where a default value of 2 for n could be used.

7.7 Constant Current Test

Variants of the isothermal test may be employed as long as it is clear that algorithms using different control parameters may produce different results.

A possible simple variation includes using a constant current value, equal to the stress current at convergence (see 6.3), i.e. $I_{test} = I_{test,\,1}$, instead of a constant power P_{test}, once target stress temperature has been reached.

NOTE In general, shorter TTFs will be measured with a constant current stress than in isothermal tests because keeping the current constant will result in an increase in the power dissipation (and temperature) during the stress phase, due to the electromigration-induced increase in resistance of the test line.

Annex A (normative) ISOT convergence algorithm

In this Annex, to examine the behavior of the convergence algorithm (see 0), it is observed that the thermal resistance $R^*_{\text{th, n}}$ and the thermal resistance intercept $T^*_{0, \text{n}}$ do not change much in the convergence phase (see Figure 8) and that they can be approximated by the values $R^*_{\text{th, test}}$ and $T^*_{0, \text{test}}$ at convergence (see 6.3.1). By these approximations, eq. (23) can be rewritten as

$$\overline{T}_{\text{n}} = T^*_{0, \text{test}} + R^*_{\text{th, test}} \times \overline{P}_{\text{n}} \tag{A.1}$$

while eq. (21) can be expressed, using the preceding relationship as well as eq. (22), as

$$\overline{P}_{\text{n}} = \frac{\overline{T}_{\text{n}} - T^*_{0, \text{test}}}{R^*_{\text{th, test}}} = \frac{T_{n-1} - T^*_{0, \text{test}}}{R^*_{\text{th, test}}} + \frac{1}{f_{\text{power}}} \times \frac{T_{\text{test}} + B_{\text{E}}/2 - T_{\text{n-1}}}{R^*_{\text{th, test}}} \tag{A.2}$$

i.e., the predicted temperature at the n-th convergence step can be calculated by

$$\overline{T}_{\text{n}} = T_{\text{n-1}} + \frac{T_{\text{test}} + B_{\text{E}}/2 - T_{\text{n-1}}}{f_{\text{power}}} \tag{A.3}$$

Table A.1 – Predicted temperature steps in the convergence phase

T_{test} = 300 °C		Convergence step number										
f_{power}	$T_{\text{staircase}}$ [°C]	1	2	3	4	5	6	7	8	9	10	11
1.0	290.00	**300.50**										
1.5	285.00	295.33	298.78	299.93	**300.31**							
2.0	280.00	290.25	295.38	297.94	299.22	299.86	**300.18**					
3.0	270.00	280.17	286.94	291.46	294.48	296.48	297.82	298.71	299.31	299.71	299.97	**300.15**

T_{test} = 350 °C		Convergence step number										
f_{power}	$T_{\text{staircase}}$ [°C]	1	2	3	4	5	6	7	8	9	10	11
1.0	340.00	**350.50**										
1.5	335.00	345.33	348.78	349.93	**350.31**							
2.0	330.00	340.25	345.38	347.94	349.22	349.86	**350.18**					
3.0	320.00	330.17	336.94	341.46	344.48	346.48	347.82	348.71	349.31	349.71	349.97	**350.15**

T_{test} = 400 °C		Convergence step number										
f_{power}	$T_{\text{staircase}}$ [°C]	1	2	3	4	5	6	7	8	9	10	11
1.0	390.00	**400.50**										
1.5	385.00	395.33	398.78	399.93	**400.31**							
2.0	380.00	390.25	395.38	397.94	399.22	399.86	**400.18**					
3.0	370.00	380.17	386.94	391.46	394.48	396.48	397.82	398.71	399.31	399.71	399.97	**400.15**

T_{test} = 450 °C		Convergence step number										
f_{power}	$T_{\text{staircase}}$ [°C]	1	2	3	4	5	6	7	8	9	10	11
1.0	440.00	**450.50**										
1.5	435.00	445.33	448.78	449.93	**450.31**							
2.0	430.00	440.25	445.38	447.94	449.22	449.86	**450.18**					
3.0	420.00	430.17	436.94	441.46	444.48	446.48	447.82	448.71	449.31	449.71	449.97	**450.15**

Annex A (normative) ISOT convergence algorithm (cont'd)

In Table A.1**,** the relationship (A.3) was calculated for four values of T_{test} (300, 350, 400, 450 ºC) and for four values of the convergence power factor f_{power} (1, 1.5, 2, 3). Typical values were chosen for the error band, i.e. B_E = 1 ºC, and for the temperature step during the staircase phase, i.e. ΔT = 10 ºC. The beginning of the convergence phase was supposed to be exactly at the temperature $T_{staircase}$, which is shown in the Table A.1, as calculated by eq. (15).

As can be seen, increasing (decreasing) the value of f_{power}, with respect to the suggested value of f_{power} = 2, lengthens (shortens) the convergence period, while the final temperature at the end of convergence phase approximates better T_{test} (see 3.6) when f_{power} is greater. In every case, should be $f_{power} > 1$.

In actual measurements, the convergence phase could begin at a temperature $T_{conv} > T_{staircase}$, depending on the preceding staircase steps. In Table A.2, the relationship (A.3) was calculated for the worst case $T_{conv} = T_{staircase} + 9.99 \approx T_{staircase} + \Delta T$: in this case the algorithm subtracts one step.

Table A.2 – Calculated temperature steps in the convergence phase

T_{test} = 300 °C			Convergence step number									
f_{power}	$T_{staircase}$ [°C]	T_{conv} [°C]	1	2	3	4	5	6	7	8	9	10
1.0	290.00	299.99	**300.50**									
1.5	285.00	294.99	298.66	299.89	**300.30**							
2.0	280.00	289.99	295.25	297.87	299.19	299.84	**300.17**					
3.0	270.00	279.99	286.83	291.38	294.42	296.45	297.80	298.70	299.30	299.70	299.97	**300.14**

T_{test} = 350 °C			Convergence step number									
f_{power}	$T_{staircase}$ [°C]	T_{conv} [°C]	1	2	3	4	5	6	7	8	9	10
1.0	340.00	349.99	**350.50**									
1.5	335.00	344.99	348.66	349.89	**350.30**							
2.0	330.00	339.99	345.25	347.87	349.19	349.84	**350.17**					
3.0	320.00	329.99	336.83	341.38	344.42	346.45	347.80	348.70	349.30	349.70	349.97	**350.14**

T_{test} = 400 °C			Convergence step number									
f_{power}	$T_{staircase}$ [°C]	T_{conv} [°C]	1	2	3	4	5	6	7	8	9	10
1.0	390.00	399.99	**400.50**									
1.5	385.00	394.99	398.66	399.89	**400.30**							
2.0	380.00	389.99	395.25	397.87	399.19	399.84	**400.17**					
3.0	370.00	379.99	386.83	391.38	394.42	396.45	397.80	398.70	399.30	399.70	399.97	**400.14**

T_{test} = 450 °C			Convergence step number									
f_{power}	$T_{staircase}$ [°C]	T_{conv} [°C]	1	2	3	4	5	6	7	8	9	10
1.0	440.00	449.99	**450.50**									
1.5	435.00	444.99	448.66	449.89	**450.30**							
2.0	430.00	439.99	445.25	447.87	449.19	449.84	**450.17**					
3.0	420.00	429.99	436.83	441.38	444.42	446.45	447.80	448.70	449.30	449.70	449.97	**450.14**

Annex B (normative) Evaluation of the damage during the initial settling time

In this Annex, a simplified method[§] is presented to account for the electromigration damage incurred during the initial settling time, t_{st}, of an isothermal test. In doing so, the actual TTF calculated from the ISOT stress period is increased by a time t_{corr} (see 6.4.1).

It is assumed that the initial settling time (i.e., the sum of the initialization, staircase and convergence periods) is approximated by a sequence of M steps, where each step (i is indexed) is at constant test conditions, i.e. temperature T_i [ºC] and current density J_i [A/cm^2], and has a duration Δt_i, depending, in turn, on the current source settling time (see 5.1), the time for resistance measurement (see 7.3), and the computer speed.

The **fractional electromigration damage**, D_i, associated to each step of the initial settling time is given by:

$$D_i = \frac{\Delta t_i}{t_{50,\,i}} \tag{B.1}$$

where the median failure time $t_{50,\,i}$, predicted for the test conditions (T_i, J_i) associated to the i-step, is

$$t_{50,\,i} = t_{50}\left(T_i, J_i\right) = A \times J_i^{-n} \times \exp\frac{E_a}{k \times \left(T_i + 273.16\right)} \tag{B.2}$$

as follows from the Black's equation (see 7.6), assuming that the activation energy, E_a, the current density exponent, n, and the constant A have the same values estimated at the target stress conditions (T_{test}, J_{test}).

By summing all the contributions (B.1), it is possible to estimate the **total electromigration damage**, D_{st}, incurred during the initial settling time

$$D_{st} = \sum_{i=1}^{M} D_i = \sum_{i=1}^{M} \frac{\Delta t_i}{A \times J_i^{-n} \times \exp\frac{E_a}{k \times \left(T_i + 273.16\right)}} \tag{B.3}$$

This damage is **equivalent** to the damage produced in a period $t_{corr} < t_{st}$, but at the target stress conditions (T_{test}, J_{test}), as during the ISOT stress phase, namely

$$D_{st} \equiv t_{corr} / t_{50,test} \tag{B.4}$$

where the median time to failure at target stress conditions $t_{50,\,test} = t_{50}\,(T_{test}, J_{test})$, is calculated by Black's equation (31). It follows that

$$t_{corr} = t_{50,\,test} \times D_{st} = J_{test}^{-n} \times \exp\frac{E_a}{k \times \left(T_{test} + 273.16\right)} \times \sum_{i=1}^{M} \frac{\Delta t_i}{J_i^{-n} \times \exp\frac{E_a}{k \times \left(T_i + 273.16\right)}} \tag{B.5}$$

is the time which can be added to the actual time to failure, TTF (i.e. the duration of the stress phase), to obtain the TTF_{corr}, corrected to account for the damage incurred during the initial settling time (see 6.4.1):

$$TTF_{corr} = TTF + t_{corr} \tag{B.6}$$

[§] M. Impronta, H. A. Schafft, private communications (2006).

Annex B (normative) Evaluation of the damage during the initial settling time (cont'd)

Table B.1 – Calculation of the fractional damage

ISOT phase	step number	t_i [s]	T_i [°C]	J_i [MA/cm^2]	Δt_i [s]	$t_{50,i} / A$	$D_i \times A$	t_{corr} [s]
T_{chuck}		*0.000*	*100.00*	*0.00*				
initialization	1	0.145	106.96	16.20	0.145	7.23E-06	2.01E+04	
	2	0.286	108.66	17.82	0.141	5.43E-06	2.60E+04	
	3	0.426	110.69	19.60	0.140	4.01E-06	3.49E+04	
	4	0.568	113.17	21.57	0.142	2.89E-06	4.91E+04	
	5	0.709	116.16	23.72	0.141	2.03E-06	6.93E+04	
	6	0.850	119.91	26.10	0.141	1.38E-06	1.02E+05	
	7	1.000	124.53	28.70	0.150	8.96E-07	1.67E+05	
	8	1.150	130.19	31.57	0.150	5.56E-07	2.70E+05	
	9	1.300	137.13	34.74	0.150	3.27E-07	4.59E+05	
	10	1.450	145.86	38.21	0.150	1.79E-07	8.39E+05	
	11	1.599	156.83	42.04	0.149	9.01E-08	1.65E+06	
	damage during initialization					$\sum D_i \times A =$	3.69E+06	2.93E-04
staircase	12	1.783	166.45	45.02	0.184	5.20E-08	3.54E+06	
	13	1.923	176.21	47.76	0.140	3.09E-08	4.53E+06	
	14	2.063	185.96	50.26	0.140	1.90E-08	7.36E+06	
	15	2.206	195.46	52.54	0.143	1.22E-08	1.18E+07	
	16	2.357	204.89	54.64	0.151	7.99E-09	1.89E+07	
	17	2.506	214.31	56.60	0.149	5.36E-09	2.78E+07	
	18	2.646	223.82	58.46	0.140	3.65E-09	3.83E+07	
	19	2.787	233.28	60.21	0.141	2.54E-09	5.56E+07	
	20	2.927	242.76	61.86	0.140	1.79E-09	7.82E+07	
	21	3.067	252.31	63.43	0.140	1.28E-09	1.09E+08	
	22	3.207	261.86	64.92	0.140	9.27E-10	1.51E+08	
	23	3.351	271.48	66.35	0.144	6.79E-10	2.12E+08	
	24	3.500	281.16	67.71	0.149	5.02E-10	2.97E+08	
	25	3.641	290.84	69.01	0.141	3.76E-10	3.75E+08	
	26	3.781	300.47	70.24	0.140	2.85E-10	4.91E+08	
	27	3.921	310.09	71.43	0.140	2.18E-10	6.41E+08	
	28	4.061	319.78	72.56	0.140	1.68E-10	8.31E+08	
	29	4.216	329.46	73.65	0.155	1.31E-10	1.18E+09	
	30	4.355	339.27	74.71	0.139	1.03E-10	1.35E+09	
	damage during staircase					$\sum D_i \times A =$	5.89E+09	0.47
convergence	31	4.496	344.92	75.29	0.141	8.96E-11	1.57E+09	
	32	4.642	347.79	75.58	0.146	8.37E-11	1.74E+09	
	33	4.792	349.21	75.73	0.150	8.09E-11	1.85E+09	
	34	4.933	349.88	75.79	0.141	7.97E-11	1.77E+09	
	35	5.075	350.19	75.82	0.142	7.91E-11	1.80E+09	
	damage during convergence					$\sum D_i \times A =$	8.74E+09	0.69
	total damage during settling time					**$D_{st} \times A =$**	**1.46E+10**	**1.16**
stress		*700.061*	*350.00*	*75.82*	*694.986*	***7.94E-11***	*8.75E+12*	

Annex B (normative) Evaluation of the damage during the initial settling time (cont'd)

Note that in the relationship (B.5):

- the knowledge of the actual $t_{50,test}$ is not needed, because the Black's constant A does not contribute;
- the optional log file (see 6.4.4) is required to calculate the fractional damage contributions D_i;
- t_{corr} is only slightly sensitive to the values selected for E_a and n, as shown ahead, so their default values are sufficient.

Also, note that, when the samples in a lot are similar, one only calculated value of t_{corr} assures a suitable compensation of the settling time damage D_{st} for the entire lot in a given ISOT experiment.

A numerical example follows, based on the ISOT test of Figure 6.

In Table B.1, the data from the ISOT optional log file, T_i, J_i, Δt_i, are used to calculate $t_{50,i} / A$ and the contributions $D_i \times A$, assuming the default values $E_a = 0.7$ eV and n = 2. The sum of these contributions gives the quantity $D_{st} \times A = 1.46^{10}$ in the next to the last row. On the other hand, it is possible to calculate (last row in Table B.1) the quantity $t_{50,\,test} / A = 7.94^{-11}$ at the target stress conditions, $T_{test} = 350$ ºC and $J_{test} = 75.82$ MA/cm^2. Finally, from eq. (B.5), it is calculated that $t_{corr} = 7.94^{11} \times 1.46^{10} = 1.16$ s , which is the time to add in eq. (B.6) to the stress phase duration to obtain $TTF_{corr} = 695 + 1.16 = 696.2$ s. It is interesting to evaluate (in the rightmost column in Table B.1) the contributions to t_{corr} given by the different ISOT phases: the contribution of the convergence phase is the most important, as expected.

In Table B.2, the slightly, monotonic dependence of t_{corr} on E_a and n is shown, by recalculating the Table B.1 and the value of t_{corr} for four possible activation energies E_a (0.65, 0.7, 0.75, 0.8 eV) and four possible values of n (1, 1.5, 2, 2.5). In these conditions, the maximum deviation from the value $t_{corr} = 1.16$ s, calculated above from the default values for E_a and n, is ± 0.07 s, which can be safely neglected in the TTF_{corr} calculation (B.6). Also when hypothesizing an experimentally very short $TTF_{corr} = 10 \times t_{corr} = 11.6$ s, the possible maximum error on the TTF_{corr} due to the unknown actual values for E_a and n, remains very small (0.07/11.6 × 100 = 0.6%).

Table B.2 – Dependence of t_{corr} on E_a and n

t_{corr} [s]		E_a [eV]			
		0.65	**0.70**	**0.75**	**0.80**
n	**1.00**	**1.23**	1.19	1.16	1.13
	1.50	1.21	1.18	1.15	1.12
	2.00	1.20	**1.16**	1.13	1.10
	2.50	1.18	1.15	1.12	**1.09**

As a consequence of being able to take into account the stress due to the initial settling time, the preceding considerations could be misinterpreted to suggest that very high stress conditions can be adopted in ISOT measurements, in an effort to reduce the duration of the test. However, this practice must be discouraged: in fact, the stress conditions are directly related to the amplitude of the temperature gradients in the structure (see 7.5), which should be kept as low as possible in isothermal tests, to obtain meaningful results.

Annex C (informative) Bibliography

[1] R. E. Jones, L. D. Smith, "A new wafer-level isothermal Joule-heated electromigration test for rapid testing of integrated-circuit interconnect", *J. Appl. Physics*, Vol. 61, 1987, pp. 4670-4678.

[2] R. S. Hijab, J. T. Yue, "The isothermal wafer level test for VLSI interconnect evaluation", *WLR Final Report*, 1992, pp. 186-198.

[3] M. Impronta, S. Farris, A. Scorzoni, "An improved isothermal electromigration test for Cu-damascene characterization", *Microelectronics Reliability*, Vol. 44, 2004, pp. 1855-1860.

[4] M. Impronta, S. Farris, A. Ficola, A. Scorzoni, "Resistance instability in Cu-damascene structures during the isothermal electromigration test", *IRW Final Report*, 2005, pp. 135-138.

[5] J. von Hagen, G. Antonin, J. Fazekas, L. Head, H. Schafft, "New SWEAT method for fast, accurate and stable electromigration testing on wafer level", *IRW Final Report*, 2000, pp. 85-89.

[6] M. Lepper, R. Bauer, A. E. Zitzelsberger, "A correlation between highly accelerated wafer level and standard package level electromigration tests on deep sub-micron via-line structures", *IRW Final Report*, 2000, pp. 70-73.

[7] D. Tibel, T. D. Sullivan, "Comparison of via/line package level vs. wafer level results", *IEEE 01CH37167, 39th Annual Reliability Physics Symp.* , 2001, pp. 194-199.

[8] T. C. Lee, D. Tibel, T. D. Sullivan, "Comparison of isothermal, constant current and SWEAT wafer level EM testing methods", *IEEE 01CH37167, 39th Annual Reliability Physics Symp*. , 2001, pp.172-183.

[9] C. E. Schuster, M. G. Vangel, H. A. Schafft, "Improved estimation of the resistivity of pure copper and electrical determination of thin copper film dimensions", *Microelectronics Reliability*, Vol. 41, 2001, pp. 239-252.

[10] J. von Hagen, H. A. Schafft, "Temperature determination methods on copper material for highly accelerated electromigration tests (e.g. SWEAT)", *IRW Final Report*, 2002, pp. 45-49.

[11] H. A. Schafft, S. Mayo, S. N. Jones, J. S. Suehle, "An electrical method for determining the thickness of metal films and the cross-sectional area of metal lines", *IRW Final Report*, 1994, pp. 5-11.

[12] J.-C. Huang, W.-T. K. Chien, C. H.-J. Huang, "Some practical concerns on isothermal electromigration tests", *IEEE Trans. on Semiconductor Manufacturing*, Vol. 14, 2001, pp. 387-394.

[13] H. A. Schafft, "Thermal analysis of electromigration test structures", *IEEE Trans. on Electron Devices*, Vol. 34, 1987, pp. 664-672.

[14] H. S. Rathore, R. G. Filippi, R. A. Wachnik, J. J. Estabil, T. Kwok, "Electromigration reliability of AlCu interconnects with W studs", *AIP Conf. Proc*., Vol. 305, 1994, pp. 165-178.

[15] J. R. Black, "Electromigration of Al-Au Alloy Films", *Proc. IRPS*, 1978, pp. 233-240.

[16] J. R. Lloyd, J. Kitchin, "The finite electromigration boundary value problem", *J. Mater. Res.*, Vol. 9, 1994, pp. 563-569.

Annex D (informative) Differences between JESD61A.01 and JESD61A

This table briefly describes most of the changes made to entries that appear in this standard, JESD61A.01, compared to its predecessor, JESD61A (May 2007). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page	Description of change
6-7	In Clause 6, the b) item dropped of page 6 creating a page 7 during conversion, this was corrected, b) was moved back to page 6.

D.1 Differences between JESD61A and JESD61

This standard, JESD61A, being a major revision on its predecessor JESD61 (April 1997), has been almost completely rewritten and/or reorganized to extend the applicability to copper-based metallizations. This table briefly points out the substantive differences, listing the new clause/subclause numbering, the corresponding numbering on the predecessor, if existing, and the main changes to the involved concepts.

JESD61A	JESD61	Differences
Foreword	2	Reorganized. The old Introduction was moved here.
Introduction	-	New. Referred to copper technology and WLR-PLR correlation.
1	1	Underlined that test structures are not specified.
2	(3)	New: applicable documents were moved in this clause.
3.1	-	New.
3.2	4	Test line distinguished from test structure, multilevel lines considered. New notes.
3.3	4	TCR: reorganized. *R-T* non-linearity cited. Includes reference temperature.
3.4	4	Thermal resistance: new definition. *T-P* non-linearity cited.
3.5	4	Target stress temperature: no substantial differences.
3.6	4	Error band: redefined.
-	4	Ambient temperature: removed definition.
-	4	Test line resistance at ambient temperature: removed definition.
-	4	Reference temperature: removed definition (now incorporated in 3.3).
-	4	Initial resistance: removed definition.
-	4	Differential thermal resistance: removed definition.
-	4	Initial resistance at target stress temperature: removed definition.
-	4	Initial power input at target stress temperature: removed definition.
-	4	Initial stress current at target temperature: removed definition.
-	4	Failure resistance: removed definition.
-	4	Cross section: removed definition (now incorporated in 3.2).
-	4	Actual time to fail: removed definition.
-	4	Convergence period: removed definition.
4	-	New: symbol list.
5.1	5.1 and 5.2	Numerical values modified.
5.2	5.3	Rewritten.
6.1	6.1	Extended. New determination of initial thermal resistance.
6.2	6.2 and 6.3	Rewritten. New temperature staircase instead of current ramp. New convergence.
6.3	6.4	Rewritten. New feedback algorithm.
6.4	6.5 and 8	Rewritten. Reporting requirements included.
6.5	6.6	Rewritten.
6.6	6.6	New example.
7.1	7.3	Rewritten. New specifications. New notes.
7.2	7.7	Rewritten. New note.
7.3	7.4	Rewritten. Details on resistance measurement added. New note.
7.4	7.2	Rewritten. Details and note on resistance instability added.
7.5	7.1	Rewritten. Multilevel structures considered.
7.6	7.8	Rewritten. Now referred to average stress current density instead of current.
7.7	7.6	Rewritten. Now referred to constant current test.
-	7.5	Removed. Settling time issues can be found in 6.1.4, 6.2.3, 6.4.1, Annex B.
-	8	Removed. Reporting requirements were moved to subclause 6.4 and redefined.
Annex A	-	New.
Annex B	-	New.
Annex C	(3)	New. Bibliography was moved in this annex and redefined.
Annex D	-	New.
Index	-	New.

Index

A

acquisition time 6, 15, 27
activation energy (E_a) 29, 32
aluminum ..... iii, 1, 2, 9, 23, 26
  test line 9, 23
ASTM F 1259M-96 ..... 1, 24

B

Black's equation 26, 29, 32, 34

C

chuck
  hot 26
  temperature (T_{chuck}) 7, 8, 18, 22, 23, 26, 27, 29
  temperature accuracy 26
  temperature display resolution 26
condition
  EXIT 17, 20, 21
  WARNING 17, 20, 21, 27
constant current test ..... iii, 29
control
  cycle time 6, 20, 27
  loop 9, 11, 12, 14, 15, 18, 19, 22
controller 6, 27
convergence
  algorithm 16, 30
  period 15, 21, 23, 31, 32
  phase 8, 9, 12, 14, 15, 16, 17, 18, 19, 22, 24, 27, 30, 31, 34
  power factor (f_{power}) 14, 15, 16, 22, 31
copper ..... iii, iv, 1, 2, 9, 23, 24, 26, 27
  damascene ..... iii, 27
  test line 2, 9, 23
correction factor
  (F_{corr}) 2, 9
  inverse ($F_{corr, inv}$) 9
correlation coefficient 12, 17, 19
cross-sectional area 2, 19, 22, 24, 28, 29
current density exponent (n) 29, 32
current multiplication factor ($f_{current}$) 9, 11, 22
current source 6, 11, 14, 27, 32
  range 14
  settling time 6, 27, 32

D

data report (*see also* log file) 22

E

electromigration damage ..... iii, 3, 7, 8, 14, 18, 19, 20, 21, 23, 32
  fractional (D_i) 32
  total (D_{st}) 32
error band (B_E) 3, 7, 8, 12, 14, 16, 18, 19, 20, 22, 31
exit-at-failure phase 21

F

failure criterion 8, 11, 17, 18, 20, 21, 22, 24
  absolute 20
  dual 20
  initialization 11
  irregular step 12, 17
  temporary 11, 17
feedback control ..... iii, 3, 6, 7, 19, 21, 27
forcing current 3, 6, 9, 11, 16, 19, 22, 27
  initial (I_1) 9, 11, 16, 19, 21, 22, 24

I

initialization
  period 11
  phase 8, 9, 11, 12, 14, 17, 22
instability 27
instrument interface 27
  IEEE-488 27

J

JEP119A ..... iii, iv, 1, 9
JESD202 ..... iii, 1, 2, 28
JESD33B ..... iv, 1, 8, 9
JESD37 ..... 1, 23
JESD61 iii
JESD87 ..... 1, 28
Joule heating ..... iii, 7, 8, 11, 26, 27, 28

K

Kelvin connections 2, 6, 27

L

log file 11, 15, 20, 21, 22, 34
  data record 22
  interval (t_{log}) 20, 22, 25

Index (cont'd)

N

number of iterations 15

O

overshoot 8, 12, 14, 16

P

power
- at target stress temperature (P_{test}) 19
- constant ..... iii, 18, 29

R

reliability
- package level (PLR) ..... iii, iv, 1, 20, 28
- wafer level (WLR) ..... iii, iv, 1, 26, 28

resistance
- after ISOT (R_{end}) 21, 22
- at chuck temperature ($R(T_{chuck})$) 8
- at convergence ($R_{test,1}$) 19, 20
- fluctuation 20
- measurement 2, 6, 27, 32

S

settling time, initial (t_{st}) 7, 8, 21, 22, 23, 24, 32, 34

staircase
- period 15
- phase 7, 8, 12, 14, 15, 17, 31

straight-line fit 3, 12, 17, 19, 25

stress
- average current density ($J_{test,\,av}$) 29
- conditions 6, 8, 21, 26, 28, 32, 34
- current at convergence ($I_{test,1}$) 19, 29
- current density (J_{test}) 19, 22, 26, 29
- phase 3, 7, 8, 9, 14, 18, 19, 20, 21, 22, 23, 25, 27, 29, 32, 34

SWEAT ..... iv, 1

T

temperature
- accuracy iv
- ambient 2, 9, 23, 26
- gradient ..... iv, 1, 2, 7, 28, 34
- mean ..... iii, 3, 7, 9, 18, 19
- oscillation 19, 20, 23, 27
- reference (T_{ref}) 2, 8, 9, 22, 24
- staircase limit ($T_{staircase}$) 8, 14, 15, 16, 31
- step, staircase phase (ΔT) 7, 12, 14, 15, 31
- target stress (T_{test}) 3, 7, 8, 12, 14, 17, 19, 26, 29
- uniformity 3, 28
- wafer 26, 27

temperature coefficient of resistance (TCR) ..... iv, 2, 7, 8, 9, 20, 22, 24, 26, 27

test line ..... iii, 2, 3, 6, 7, 8, 9, 11, 12, 15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29

test structure ..... iv, 1, 2, 3, 6, 7, 23, 27, 28
- multilevel 20, 28
- single-level 2, 28

thermal conductance 3

thermal model ..... iv, 7

thermal resistance
- (R^*_{th}) ..... iii, 3, 7, 8, 9, 11, 12, 14, 15, 16, 17, 18, 19, 20, 23, 25, 27, 28, 29, 30
- initial ($R^*_{th,1}$) 11, 12, 17
- intercept (T^*_0) 3, 12, 15, 16, 17, 19, 22, 25, 30

thermal response time 27

time to failure (TTF) 6, 8, 21, 22, 23, 25, 28, 29, 32
- corrected (TTF_{corr}) 21, 32, 34
- median (t_{50}) 29, 32, 34
- normalized (TTF_{norm}) 29

time-to-failure correction (t_{corr}) 8, 21, 32, 34

V

vias 1, 2, 20, 24, 27, 28

voltage compliance (V_C) 6, 11, 14

voltage taps (*see also* test structure) 2, 11, 17, 20

voltmeter 6, 11, 14, 23, 27
- conversion time 6, 27
- delay 27
- input filter 6, 27
- integration time 6, 27
- range 11, 14
- reading rate 6, 27

W

wafer prober (*see also* chuck) iii

weak population 23

Standard Improvement Form **JEDEC** **JESD61A.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
2500 Wilson Blvd. Suite 220
Arlington, VA 22201-3834
Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, paragraph number _____

☐ Test method number _____ Paragraph number _____

The referenced paragraph number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC